

DESIGN AN AGING-AWARE RELIABLE H-MULTIPLIER

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ABSTRACT

*This paper presents the design an H-Logic[H.L] multiplier for 32*32bit number multiplication. Modern computer system is a dedicated with very high speed unique multiplier. Therefore, this paper presents the design an H-Logic multiplier. The proposed system generates M, N and X blocks. By extending bit of the operands and generating an additional product the H-Logic multiplier is obtained. Multiplication operation is performed by the H-Logic is efficient with the less area and it gives the reduces delay i.e., speed is increased.*

Keywords: H.L, H- level logic unit, partial products

I. INTRODUCTION

Multiplication is a basic fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume operating considerable power. Therefore low-power multiplier design has been an important part in low-power VLSI system design. We have extensive work on low-power multipliers at technology, physical, circuit and logic levels. A system's performance is generally depends on the basically performance of the multiplier because the multiplier is generally the slowest element in any system.

II. LITERATURE SURVEY

Multiplication operation has been paid most attention by researchers, because addition is simply bitwise XOR operation between two field elements, and the more complex operations, inversion, can be carried out with a few multiplications. In [21], an LSD-first multiplier with lower area-time complexity has been proposed using a new method for the accumulation in which XOR gates and D flip-flops (FFs) have been replaced by T FFs and feedback loops have been eliminated. In [30], a multiple-bit serial-parallel multiplier has been proposed. One operand is decomposed recursively and the other operand is prerduced hierarchically. The multiplier has higher area complexity compared with some of the existing multipliers; however, it has lower critical path delay, which results in lower area-time complexity.

A low-complexity digit-serial SPB multiplier using the proposed(b, 2)-way Karatsuba decomposition has been proposed. The (4, 2)-way and (6, 2)-way Karatsuba-based digit serial multipliers have been implemented and compared with the existing SPB multiplier. The Karatsuba-based digit-serial SPB multiplier shows lower area complexity, less area-delay product, and less energy consumption compared with the existing SPB multiplier.

III. PROPOSED TECHNIQUE

In this paper, an H- technique is adopted in design of a digit-serial PB multiplier. To the best of our knowledge, a factoring method has not been reported in the literature being used in the design of a finite field multiplier at an architectural level. A logic gate substitution technique is also used in our design to reduce the internal power consumption of the proposed H- multiplier.

The synthesis results show that our new design has both the lowest area consumption and the less memory used consumption among several similar existing works.

A column-bypassing multiplier is an improvement on the normal array multiplier (AM). The multiplier array consists of $(n-1)$ rows of carry save adder (CSA), in which each and every row contains $(n-1)$ full adder (FA) cells. Each FA in the CSA array has two outputs: 1) the sum bit goes down and 2) the carry bit goes to the lower left FA. The last row is a ripple adder for carry propagation.

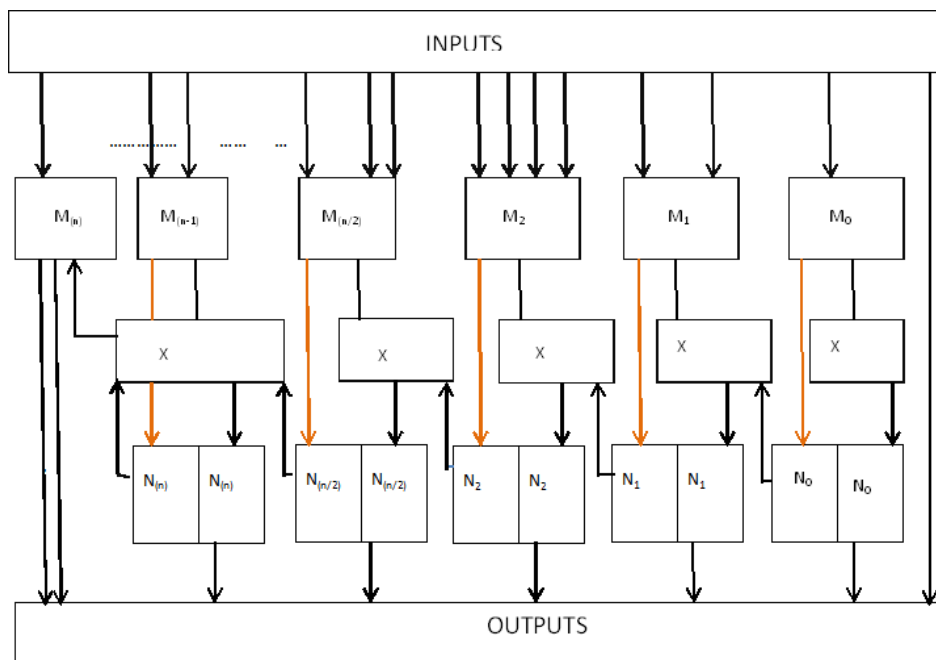


Fig. 1 4 x 4 HIGH PERFORMANCE H-LOGIC MULTIPLIER

IV. PROPOSED SYSTEM

The gates in the H-Logic [H.L] multiplier are always active regard of input logics. In H-Logic[H.L] multiplier design is proposed in which the operations are disabled if the corresponding bit in the multiplicand is 0. Fig. 1 shows a $N \times NH$ -Logic[H.L] multiplier, it can be seen that the

M_0, M_1, \dots, M_n done their operations and the outputs are passed to interconnected

To evaluate the complexities of H-MUL arithmetic hardware, circuit complexity is usually presented by the number of FFs, two-input AND gates, two-input XOR gates, and MUXs. In estimation of critical path delay is used to refer to as the delay caused by a two-input AND gate, a two-input or gate, a two-input XOR gate, a 2-to-1 multiplexer, a D FF, and a T FF, respectively.

Block and N-Block simultaneously. Depends on the preference of operation the H- level logic gives the N-block output to interconnected block and vice versa.

Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit. The above fig. 1 shows the 4*4 high performance H-Logic multiplier reduced the timing waste occurring in traditional circuits that use the critical path cycle of an execution cycle period. The basic concept is to execute a shorter path using H-logic. Since most paths execute in a cycle period that is very smaller than the critical path delay. The same architecture is extended up to 32*32 bits.

H-Logic widely been adopted in multipliers since it can reduce the number of partial product rows to be added, thus reducing the size and enhancing the speed of the reduction tree. The least significant bit position of each partial product is rowen coding, leading to an irregular partial product array and a complex reduction tree.

Therefore, the H-Logic multipliers with partial product array produce a very high speed.

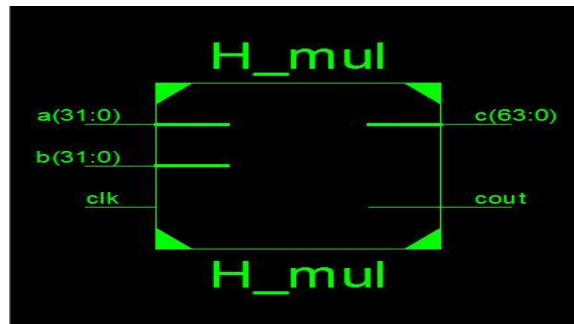


Fig. 2 R.T.L Schematic

The above fig. 2 shows the R.T.L schematic of high performance H-Logic multiplier and fig. 3 shows the technical schematic one of the LUT block of high performance H-Logic multiplier.

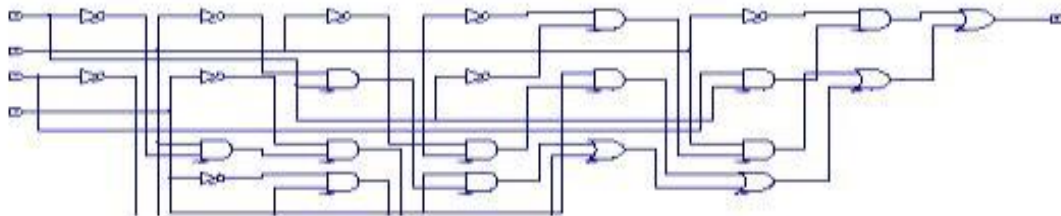


Fig. 3 LUT in technical Schematic

The below figure 4 shows the output waveform of 32*32 bit H-Logic multiplier.

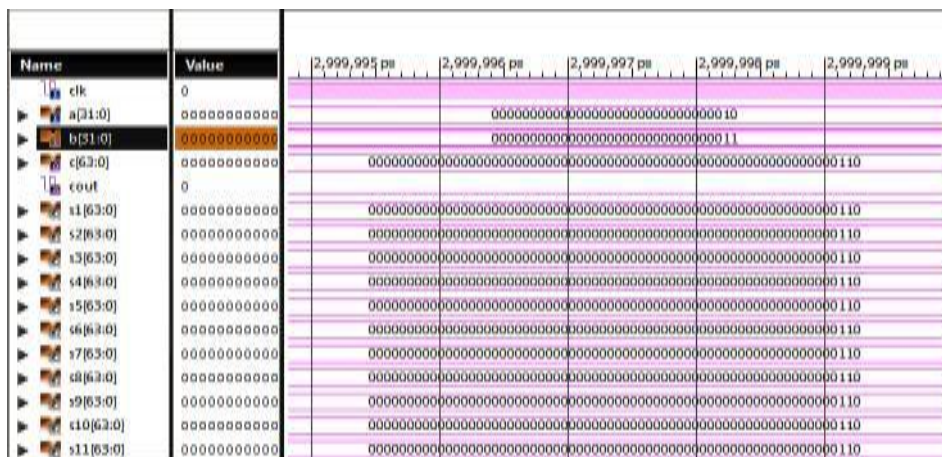


Fig. 4 OUTPUT Waveforms

The below table 1 shows the comparison of existed system and proposed system with area and delay

System/parameter	Area[kb]	Delay[ns]
Existed System	382256	410
Proposed system	366700	102.80

Table.1 comparison table

The above comparison table shows that area of the proposed system is less compare with the existed system and delay is also efficient.

V. CONCLUSION

The H - technique has been adopted for a new architecture level design that minimizes the switching activities and consequently, reduces the power consumption of a digit-serial multiplier. The logic gate substitution technique has also been utilized to further reduce the power consumption of the digit-serial H-multiplier. Moreover, the area complexity of the finite field multiplier has been reduced.

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