International Journal of Innovative Research in Science and Engineering
Vol. No.2, Issue 01, January 2016
www.ijirse.com
ISSN: 2454-9665

DESIGN OF VEDIC MULTIPLIER USING HIGHER ORDER COMPRESSOR TO INCREASE THE SPEED AND AREA

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ABSTRACT

Nowadays the high speed processors and low area designs have the most demand with the advance new technology in the VLSI and communication fields. Multiplier is one of the main integral parts in the processor design. The high speed multiplier architecture should need the required delay. So in this paper we are designing a high speed Vedic multiplier. For high speed implementation we are using 4:2 compressors and 7:2 compressors for adding the partial products. Simple we are designing a compressor based Vedic multiplier which is having two times faster than other multiplication methods and also having less delay. This design area and delay implemented by the XILINX ISE 13.2 i with Verilog HDL.

Keywords: High Speed Multiplier, 4:2 and 7:2 Compressor, Urdhva-Triyakbhayam, Vedic Mathematics.

I. INTRODUCTION

The speed of a processor significantly relies on upon its multiplier's execution. This thusly expands the interest for fast multipliers, in the meantime remembering low area and power utilization. In the course of the last few decades, a few new architectures of multipliers have been outlined and investigated. Multipliers in view of the Booth's what's more, modified Booth's calculation is entirely mainstream in cutting edge VLSI plan yet join their own arrangement of burdens. In these calculations, the increase process includes certain operation which makes the design complex and large. The transitional stages will test the speed a few examinations, augmentations and subtractions which decrease the speed exponentially with the aggregate number of bits present in the multiplier and the multiplicand. Since velocity is our major concern, using such sort of architectures is not a practical approach since it includes a few tedious operations.

So as to address the impediments regarding speed of the aforementioned stspeedgies, is investigated another way to deal with multiplier configuration taking into account old Vedic Arithmetic. Vedic Mathematics is an antiquated and famous approach which goes about as an establishment to tackle a few numerical difficulties experienced in the present day situation. Vedic Mathematics existed in antiquated India and was rediscovered by a well-known mathematician, Sri Bharati KrishnaTirthaji. He bifurcated Vedic arithmetic into 16 straightforward sutras (formulae). These Sutras manage Arithmetic, Algebra, Geometry, Trigonometry, and

Analytical Geometry and so on. The straightforwardness in the Vedic arithmetic sutras clears route for its application in a few noticeable areas of designing like Sign Processing, Control Engineering and VLSI.

One of the highlights of the Vedic maths methodology is that the computation of all the partial products required for increase multiplication, are acquired well ahead of time, much before the real operations of multiplication start. These fractional items are then summed based the Vedic maths calculation to get the last item. This thusly prompts a fast way to deal with perform increase. In this paper, we investigate a novel technique to further upgrade the velocity of a Vedic science multiplier by supplanting the current full adders what's more, half adders of the Vedic science based multipliers with compressors. Compressors, in its few variations, are logical circuits which are equipped for including more than 3 bits at a time instead of a full adder and fit for performing this with a lesser door include and higher velocity examination with a proportional full adder circuit.

II. VEDIC MULTIPLIER DESIGN DESCRIPTION

2.1 Vedic Maths - Urdhwa Tiryakbhyam Sutra

Vedic Mathematics can be isolated into 16 unique sutras to perform numerical computations. Among these the UrdhwaTiryakbhyam Sutra is one of the most profoundly favoured calculations for performing multiplication. The calculation is sufficiently equipped to be utilized for the increase of numbers and in addition parallel numbers. The expression "UrdhwaTiryakbhyam" started from 2 Sanskrit words Urdhwa and Tiryakbhyam which is represented as a 'horizontal and "vertically" separately. The primary point of interest of using this calculation in examination with the existing increase systems, is the way that it uses just intelligent "AND" operations, half adders and full adders to complete the multiplication calculation. Likewise, the fractional items required for multiplication is produced in parallel what more; apriority to the genuine expansion in this way is sparing a considerable measure of handling time.

Give us a chance to consider two 8 bit numbers X7-X0 and Y7-Y0, where 0 to 7 speak to bits from the Least Significant Bit (LSB) to the Most Significant Bit (MSB). P0 to P15 speak to every piece of the last figured item. It can be seen from mathematical statement (1) to (15), that P0 to P15 are ascertained by adding incomplete items, which are ascertained already utilizing the sensible AND operation. The individual bits acquired from mathematical statements (1) to (15), thusly when connected produce the last result of augmentation which is portrayed in (16).The carry bits created amid the computation of the person bits of the last item are spoken to from C1 to C30. The carry bits created in (14) and (15) are disregarded since they are pointless.

$$P0 = A0 * B0 \quad (1)$$

$$C1P1 = (A1 * B0) + (A0 * B1) \quad (2)$$

$$C3C2P2 = (A2 * B0) + (A0 * B2) + (A1 * B1) + C1 \quad (3)$$

$$C5C4P3 = (A3 * B0) + (A2 * B1) + (A1 * B2) + (A0 * B3) + C2 \quad (4)$$

$$C7C6P4 = (A4 * B0) + (A3 * B1) + (A2 * B2) + (A1 * B3) + (A0 * B4) + C3 + C4 \quad (5)$$

$$C10C9C8P5 = (A5 * B0) + (A4 * B1) + (A3 * B2) + (A2 * B3) + (A1 * B4) + (A0 * B5) + C5 + C6 \quad (6)$$

$$C13C12C11P6 = (A6 * B0) + (A5 * B1) + (A4 * B2) + (A3 * B3) + (A2 * B4) + (A1 * B5) + (A0 * B6) + C7 + C8 \quad (7)$$

$$C19C18C17P8 = (A7 * B1) + (A6 * B2) + (A5 * B3) + (A4 * B4) + (A3 * B5) + (A2 * B6) + (A1 * B7) + C10 + C12 + C14$$

C22C21C20P9 = (A7 * B2) + (A6 * B3) + (A5 * B4) + (A4 * B5) + (A3 * B6) + (A2 * B7) + C13 +C15 + C17 (10)

C25C24C23P10 = (A7 * B3) +(A6 * B4) + (A5 * B5) + (A4 * B6) +(A3 * B7) + C16 + C18 + C20 (11)

C27C26P11 = (A7 * B4) + (A6 * B5) + (A5 * B6) + (A4 * B7) + C19 + C21 + C23 (12)

C29C28P12 = (A7 * B5) + (A5 * B6) + (A5 * B7) + C22 + C24 + C26 (13)

C30P13= (A7 * B6) + (A6 * B7) + C25 + C27 + C28 (14)

P14 = (A7 * B7) + C29 + C30 (15)

P15= (A7 * B7) (16)

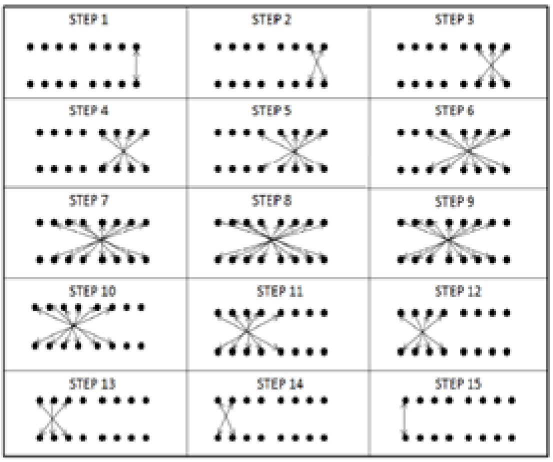

Fig 2.Pictorial representation of Vedic algorithm

Fig.2 graphically outlines the regulated system for multiplying two 8 bit numbers utilizing the UrdhwaTiryakbyam Sutra. The dark circles demonstrate the bits of the multiplier and multiplicand, and the two-way bolts demonstrate the bits to be multiplied with a specific end goal to touch base at the individual bits of the last item. The equipment building design of the 8x8 Urdhwa multiplier has been planned and appeared in Fig. 2. As said before, the partial products items acquired are included with the assistance of full adders and half adders. It can be seen, from mathematical statement (1) to (16), that in couple of comparisons there is a need of including more than 3 bits at once. This prompts extra equipment and extra stages, subsequent to the full adder is equipped for including just 3 bits at once. In the following area two unique sorts of compressor architectures are investigated which help with including more that 3 bits at once, with lessened structural engineering and expanded productivity as far as rate.

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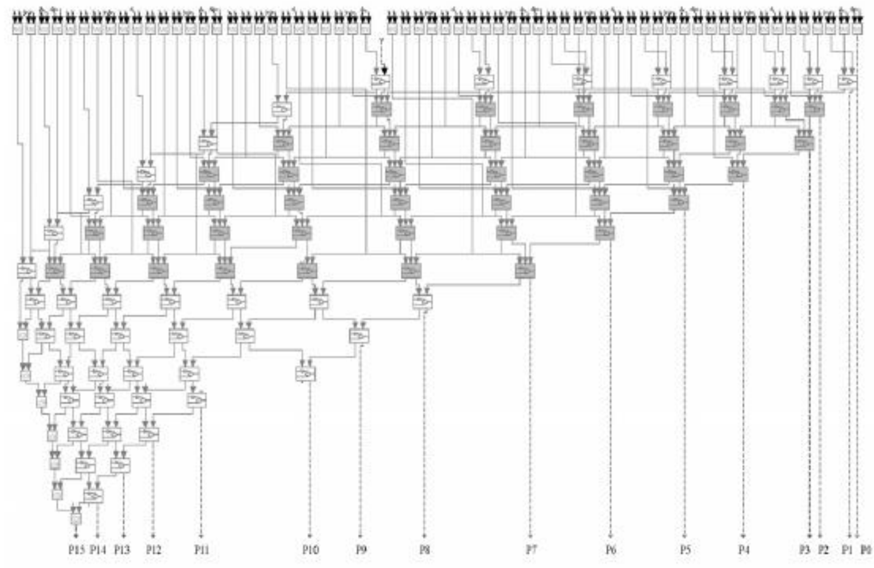

Fig 2.1Hardware architecture of Urdhva Tiryakbhyam multiplier where the gray colored blocks represent the full adders and the white colored blocks represent the half adders

2.2 Compressor Adder

A compressor adder is a consistent circuit which is utilized to enhance the computational pace of the summing of 4 or more bits at once. Compressors can effectively supplant the blend of a few half adders and full adders, in this manner empowering fast execution of the processor which joins the same. The compressor adder utilized as a part of this paper is a 4:2 compressor adder. A great deal of examination in the past has been did on the same. This has been explained beneath. An examination of the 4:2 compressors with a proportionate circuit, utilizing full adders and half adders has likewise been given beneath.

A. 4:2 Compressor Adder

Fig 2.2 4:2 Compressor block diagram

A 4:2 compressor as appeared in fig.2.2 .is equipped for adding 4 bits and one carry, thus creating a 3 bit output. The inside building design of the same has been show in fig.4. It can be plainly seen, the proper process is small in correlation with an equal circuit to include 5 bits utilizing full adders and half adders. For the purpose of correlation, the comparable circuit to include 5 bits has additionally been appeared in Fig. 5.

Let us a choose to consider the propagations delay of an gate to be tp. It is surely understood that a full adder has an aggregate proliferation delay of 2tp and a half adder has a spread delay of tp. Considering this, the

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www.ijirse.com
IJIRSE
ISSN: 2454-9665

aggregate propagation delay of a 4:2 adder utilizing full adders what's more, half adders can be computed as 5tp and can be seen in Fig.5. Then again, it can be seen from Fig. 4. that the proliferation postponement of a 4:2 compressor stays just 3tp. Along these lines, a 66.6% expansion in rate can be recorded in examination with a comparable circuit made of full and half adders, turned out to be a very effective building design for expansion.

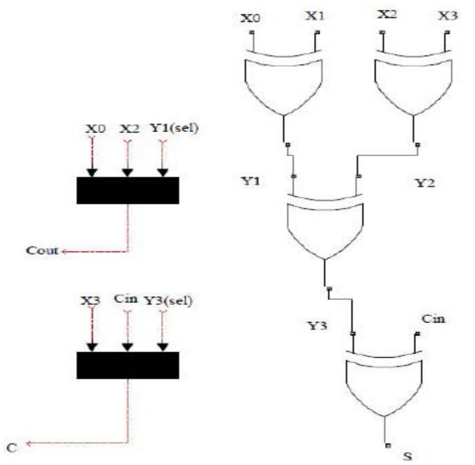

Fig 2.3 Gate level diagram of 4:2 Compressor

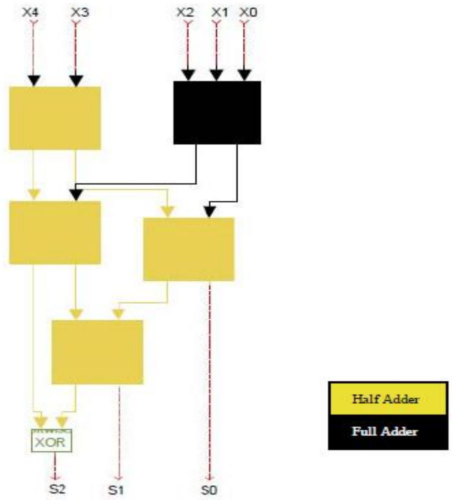

Fig2.4 Compressor using full adders and half adders

Keeping in mind the end goal to include more than 5 bits at once, yet another compressor structural planning – the 7:2 compressor adder could be utilized and this is clarified as a part of subtle element underneath.

B. 7:2 Compressor Adder:

Like its 4:2 compressor partner, the 7:2 compressor as appeared in Fig. 6., is fit for including 7 bits of data and 2 carry's from the past stages, at once. In our execution, we have planned a novel 7:2 compressor using two 4:2 compressors, two full adders and one half adder. The building design for the same has been appeared in Fig. 7. As said before, since the 4:2 compressors demonstrates a huge increment in velocity by around 66.6%, using the same in this structural engineering would enhance the effectiveness as restricted to a customary methodology of including nine bits at a time utilizing just full adders and half adders. This prompts a awesome ad lib in rate of the processor. Through experimentation on a Xilinx Spartan-3e FPGA, it was found that the novel 7:2

compressor adder building design presented here is 1.05 times quicker than a customary methodology. This result legitimizes the need of using this compressor in our plan.

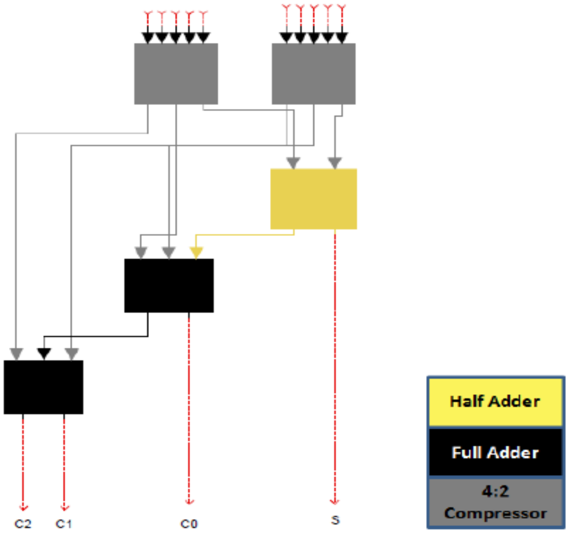

Fig 2.5 7:2 Compressor using 4:2 Compressor adder

III. PROPOSED COMPRESSOR WITH VEDIC MULTIPLIER

3.1 Higher Order Compressors

Several 4-2 and 5-2 compressor architectures were reported so far. the main downside associated with those conventional compressors is that the result generated isn't in right binary form and one extra half adder/ full adder is needed to get the very last outcomes, thereby increasing the location and energy dissipation. Furthermore, because of choppy delay profiles of the outputs coming back from distinctive enter paths; plenty of system faults are generated. to overcome those problems associated with the traditional compressors, better order compressors proposed were used inside the layout. Those compressors were designed as counter of „1"s on the input bits. full adder itself is a counter of one"s at its enter as illustrated in desk I. consequently, full adder acts as three-2 compressor. The similar good judgment may be used to design the better order compressor circuits..

Table 3.4.1 Full adder as a counter

Number of 1's at the input	Output		Equivalent decimal value
	Carry	Sum	
Zero	0	0	0
One	0	1	1
Two	1	0	2
Three	1	1	3

Table 3.4.2 4-3 compressor as a counter

Number of 1's at the input	Output			Equivalent decimal value
	C3	C2	C1	
Zero	0	0	0	0
One	0	0	1	1
Two	0	1	0	2
Three	0	1	1	3
Four	1	0	0	4

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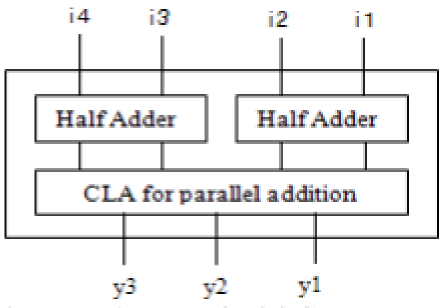

Fig.3.4.1 Block diagram of a 4-3 Compressor

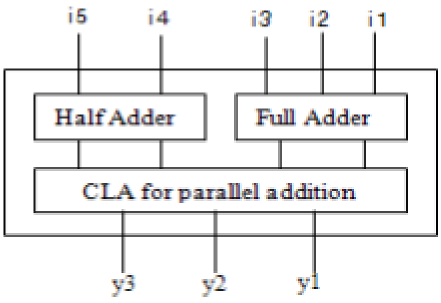

Fig.3.4.2 Block diagram of a 5-3 Compressor

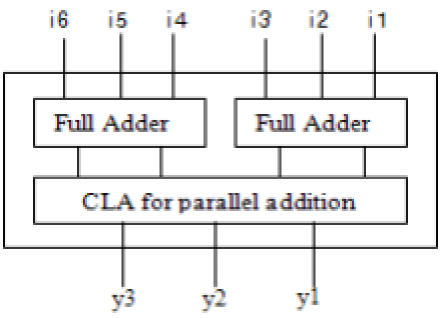

Fig.3.4.3 Block diagram of a 6-3 Compressor

The block diagrams of four-3, five-three and 6-3 compressor incorporates three sub-devices: adder gadgets and a convey appearance ahead adder (CLA) unit for parallel addition of the outputs of the adder gadgets. The 7-three compressor is applied the usage of 4-3 compressor, a complete adder and a CLA unit.

3.2 Proposed Vedic Multiplier

In the sooner compressor primarily based Vedic Multiplier, a large quantity of ranges are required to feature the partial products to acquire the final effects. The four-2 and 7-2 compressors are applied most effective in the first ranges of the multiplier whilst the following eleven stages employ only full adder and 1/2 adder thereby increasing the discount degrees to thirteen .This ends in improved region and energy intake. within the proposed multiplier structure, the better order compressors were used intelligently so that the partial merchandise are added in only two tiers to attain the very last result and hence giving an area green and low power ingesting design. Additionally, compressors and adders are employed such that minimum range of outputs is generated. For instance in column 5, there are 7 partial merchandise to be delivered. Those can be brought the usage of a four-3 compressor and a full adder thereby producing five output bits. But as opposed to this a 7-3 compressor has been used that allows you to generate most effective 3 output bits. The identical technique has been utilized for different columns as well

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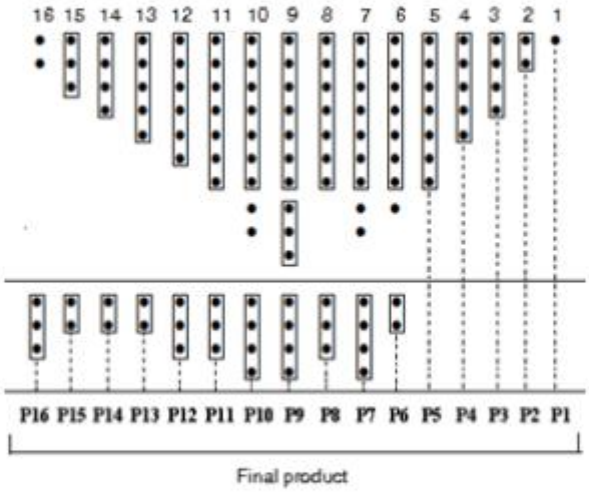
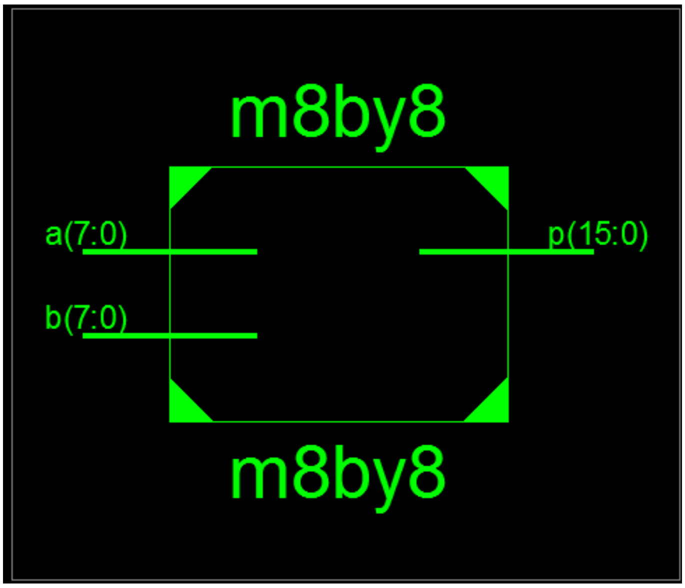


Fig 3.2.1 Proposed Vedic Multiplier Reduction

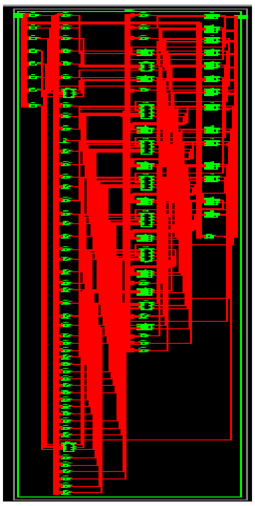
The following segment examines a novel way to deal with join the productivity of the compressor architectures presented previously with the current Vedic science approach for increase.

IV. SYNTHESIS AND SIMULATION RESULTS

In this project we are designing compressor based Vedic multiplier. The existed compressors are taking much area to improve the performance of the existing design, We have employed Novel design of compressors which generates the actual sum in binary form without requiring the additional area overhead. The proposed compressors are designed in Verilog HDL. The design is synthesised in Xilinx ISE 13.2i. The synthesis reports are presented below.



Internal structure of Top module:



Synthesis results:

m8by8 Project Status			
Project File:	vediccompressor.xise	**Parser Errors:**	No Errors
Module Name:	m8by8	**Implementation State:**	Synthesized
Target Device:	xc7a30t-3csg324	• **Errors:**	No Errors
Product Version:	ISE 13.2	• **Warnings:**	No Warnings
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	95	21000	0%
Number of fully used LUT-FF pairs	0	95	0%
Number of bonded IOBs	32	210	15%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon 9. Nov 17:10:40 2015	0	0	0
Translation Report					
Map Report					

```
Delay:               8.743ns (Levels of Logic = 16)
  Source:            a<2> (PAD)
  Destination:       p<14> (PAD)

  Data Path: a<2> to p<14>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O            17   0.001   0.453  a_2_IBUF (a_2_IBUF)
     LUT2:I0->O            1   0.097   0.683  w<2><0>1 (w<2><0>)
     LUT6:I1->O            3   0.097   0.566  n3/cout1 (c<2>)
     LUT4:I0->O            2   0.097   0.384  n4/n2/cout1 (s<4>)
     LUT6:I4->O            2   0.097   0.384  n6/n2/Mxor_s_xo<0>1 (s<6>)
     LUT5:I3->O            2   0.097   0.384  n8/cout1 (c<7>)
     LUT5:I3->O            3   0.097   0.521  n11/cout1 (c<11>)
     LUT6:I3->O            2   0.097   0.516  n15/n5/cout1 (c<16>)
     LUT4:I1->O            2   0.097   0.383  n17/cout1 (c<19>)
     LUT5:I3->O            3   0.097   0.521  n20/cout1 (c<23>)
     LUT6:I3->O            2   0.097   0.697  n24/n2/Mxor_s_xo<0>1 (s<30>)
     LUT6:I0->O            3   0.097   0.521  n25/Mxor_s_xo<0>1 (s<32>)
     LUT6:I3->O            3   0.097   0.521  n27/n2/Mxor_s_xo<0>1 (s<34>)
     LUT6:I3->O            4   0.097   0.570  n29/cout1 (c<33>)
     LUT6:I2->O            1   0.097   0.279  n31/Mxor_s_xo<0>1 (p_13_OBUF)
     OBUF:I->O                 0.000          p_13_OBUF (p<13>)
    ----------------------------------------
    Total                      8.743ns (1.359ns logic, 7.384ns route)
                                       (15.5% logic, 84.5% route)
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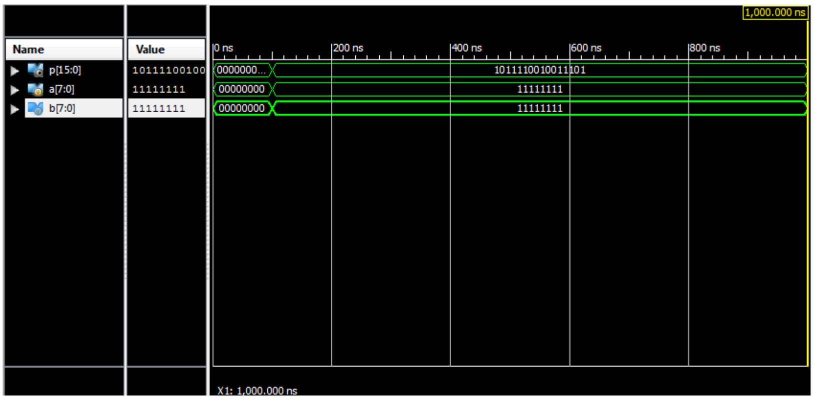
www.ijirse.com
ISSN: 2454-9665

Simulation results:



V. CONCLUSION

In this paper We have implemented high order definite compressor based Vedic multiplier using Verilog hardware description language. And synthesis and simulation can be done by using Xilinx ISE 13.2 version software. The proposed compressor based Vedic multiplier have less hardware complexity, high speed and low power dissipation and less day compare with existed binary multiplication that was shown in the above results.

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AUTHOR DETAILS

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