

DESIGN OF DOUBLE EDGE AND SINGLE EDGE TRIGGERED FLIP FLOP WITH ENHANCED PULSE FEED THROUGH SCHEME FOR LOW POWER OPERATIONS

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ABSTRACT

In this paper we are proposing the a pulse triggered flip flop and Double edge triggered flip flop designs with single feed through scheme . The flip flops are the basic storage elements in the all memory based electronic equipment's. Memory is the collection of registers such registers are made of the flip flops. To optimize the performance of the flip flop, we are aimed to reduce the leakage power, the existing designs in literature will have longer discharging path between output node to the ground. To avoid this problem the pulse generator circuit will be using to reduce the width of the clock, such that discharging path will be reduced consumed power will saved. The presented circuits are pre simulated using TSMC025nm technology. The simulated results proved that DET and Edge triggered flip flop using pulse generated circuits having low power performances with compared to the existing design.

Keywords: *TSPC,Switching power, Pulse triggering, DET*

I. INTRODUCTION

The flip flops are the basic storage elements that will be used in all kind of electronic designs. In current all designs are using collection flip flop modules in them. The Flip flop collection may be such as shift registers, fifo and Register set or register files. The power consumption of digital design is due to the modules in it and also due to the clock system. The clock system that comprises of clock generator, clock distributing networks and storage elements. This consumes almost 50% of the total power consumed by the design hence the flip flops will also play a vital role in the power consumption. Several architectures are presented in the literature for flip flops. All of such designs will have two latches in it which makes design area is high and higher propagation delay. To reduce area and delay we have approached pulse triggered flip flop which is a circuit that can have single latch and pulse generation circuit. The pulse generation circuit will generate pulses from the clock and fed to the latch. The pulse generation circuit will be used to generate strobe signal, latch is used for data storing. The single latch structure made attractive in less area and high toggle rate which leads to the high speed designs. Even though it's facilitating all features still it needs delicate pulse width control over pulse generation circuit such that it will cooperate with the process variation in the designs. It will also functions as an edge triggered

flip flop when it's having widths are very near. In the presented paper we have introduced the am mechanism which feeds the input signal directly to the output node for high speed data transfer. This is actually implements a pass transistor to drive the input signal to the node. We also implemented double edge triggered which has two latches but better speed performances over past design. These all are new designs of flip flops.

II. EXISTING DESIGN IN LITERATURE

The pulse triggered flip flops may be classified based on the pulse generation circuit that present in the flip flop. If the pulse generation circuit in existed inside of the complex latch design then we can call it as implicit PFF, the pulse generation circuit is a part from the latch they we can call it as explicit type P-FF. Implicit type P-FF don't need any extra circuitry so we can say its consumed less power where as in Explicit FF will need two additional circuit hence more power will be consumed. Even though the implicit is power economical it suffers from the longer discharging path which makes speed inefficient. The separate circuits for latch and logic will make the design power inefficient but it adopts good speed advantage. We will concentrate on the explicit PFF to reduce its power consumption. This is achieved by the group flip flop may use single pulse generation circuit such that power will be saved. Let we discuss few designs of the explicit type PFF. The basic design in Ep-DCO flip flop which may also called as data close to output FF. The circuit diagram shown in fig 2.1, the pulse generation circuit is constructed based on the Nand Logic. The inverters I3, I4 are used to latch the data, Inverters I1, I2 re used to hold the output node X. The path delay of the pulse circuit is measured by the three inverters present pulse generator. This circuit will have problem of node X will discharge for very rising of edge of the clock when input to the circuit is static '1' which leads to switching power consumption.

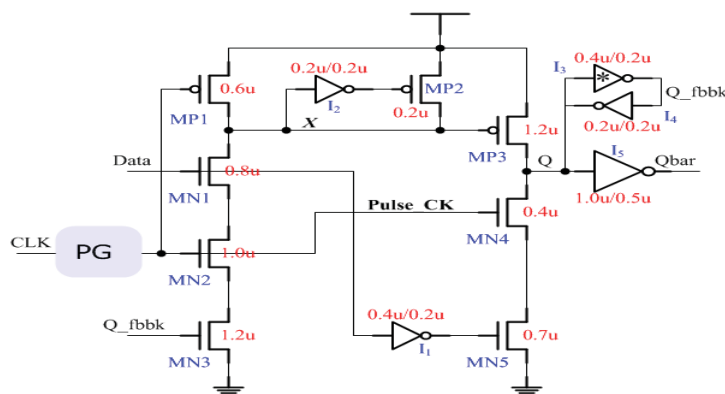


Fig 2.1 Ep-dco

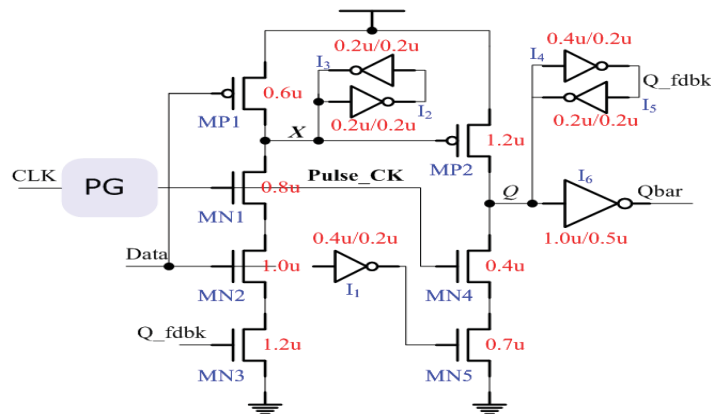


Fig 2.2 CDFF

To avoid such problems we have considered the solution as conditional precharge, conditional discharge, conditional enhancement schemes. Let see the conditional discharge based FF contains the extra transistor connected to the circuit controlled by the Q_feed back. This will avoid the discharging of node X at input '1'. The node hold logic will be more simplified by placing a PMOS transistor with the inverter. Small enhancement made to the circuit will make it as static CD FF. The Static implementation of the latch will accomplish Sdff.

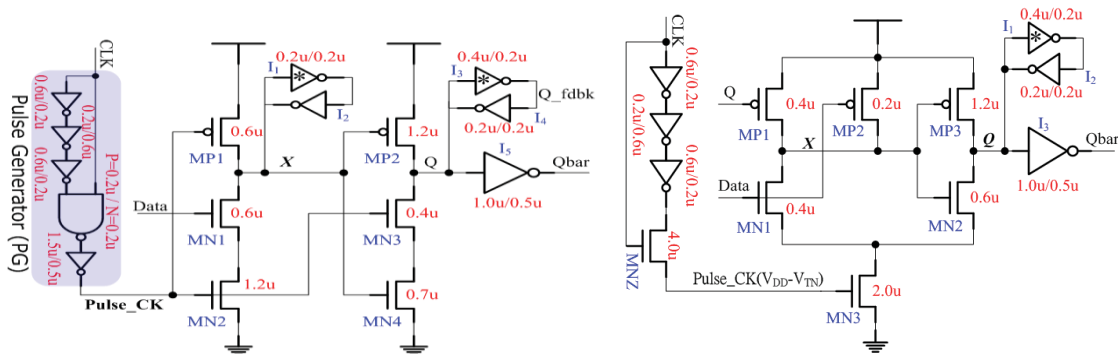


Fig 2.4 MHL FF

These two will suffers from delay in between data to output by the transistor MN1-MN3. To avoid this delay we need extra pull up network which makes additional area and power. The modified hybrid flip flop is proposed is modified hybrid flip flop. This also implements the static latch structure. In this circuit the hold logic for node x will be removed, simple a NMOS transistor with output Q will monitors the level at node X. Due to its simple structure it faces two problems are node X will be floating certain times and other one is node X will not pre discharge which makes loner 0 to 1delay such that degraded clock pulses will be applied to MN3 transistor which makes to draw extra dc power.

III. PROPOSED FLIP FLOP DESIGN

The proposed flip flop will avoid the drawbacks that are associated with the existing flip flops. The delay between the data and output Q is avoided by employing signal feed through scheme. The design also adopts the static latch with conditional discharge architecture will be employed to avoid continues transition at node X.

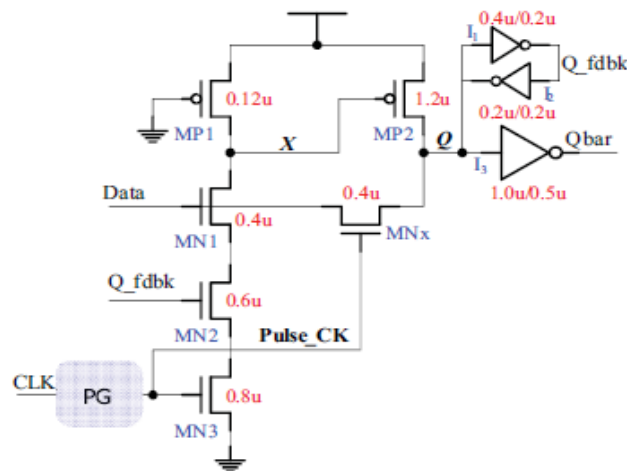


Fig 3.1 proposed flip flop with signal feed through scheme

The circuit contains ground will be the first stage of the circuit, which implements as pseudo Nmos logic style which saves the keeper logic of node X. The transistor MNx is employed between input and output. The transistor which is controlled by the pulse clock. This pulse controlled transistor with MP2 will form second stage of the circuit. The path will leads to driving of output Q with influence of the input. The second stage pull down network will be completely removed such that the MNx transistor will provide discharging path between the input and output. The transistor MNx performing two roles are the driving the output and discharging the output depend upon the value of the transition. If data transition between 0 and 1, it will be driving the Q else data transition between 1 and 0 it will be discharging the Q. The circuit will have less area due to the avoiding of keeper logic, pull down network in second stage, and control logic but having one extra NMOS pass transistor is used in this network. This extra transistor which facilitates the signal feed through scheme which avoids delay between 0 to 1 such that to avoid confusion between the rise and fall time.

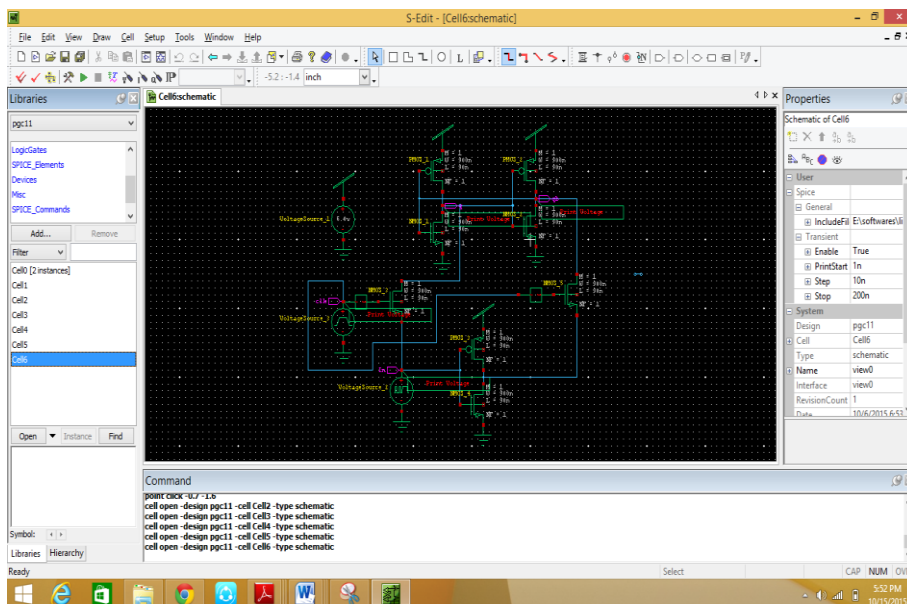


Fig 3.2 DET with signal feed through scheme

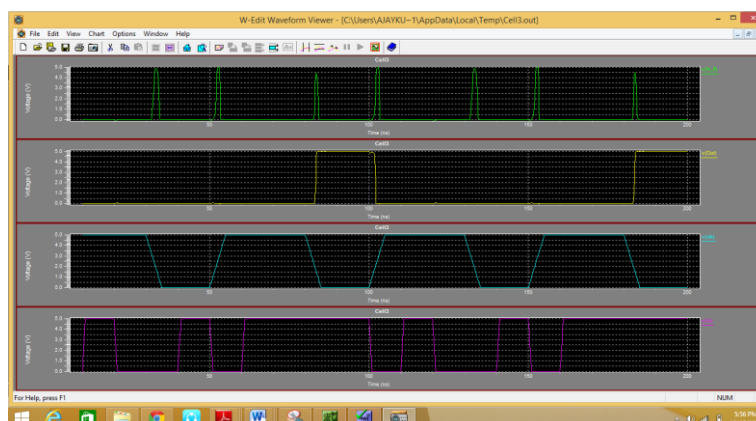
The proposed flip flop functions as like regular flip flop, when clock pulse raised, when the input voltage and Q voltage at the same level there may be no data transitions, current will be passed to the MNx transistor makes no driving output since both are at same level. When the input and Q feedback will have complementary values, the node voltage is off at that time there will be no transitions at any internal nodes. If there may be any transitions in data from 0 to 1 leads to the node X will be discharged to make turn the MP2 transistor. That makes the output will be high. The proposed signal feed through schemes which give rise from the input through the pass transistor MNx that effectively reduces the delay.

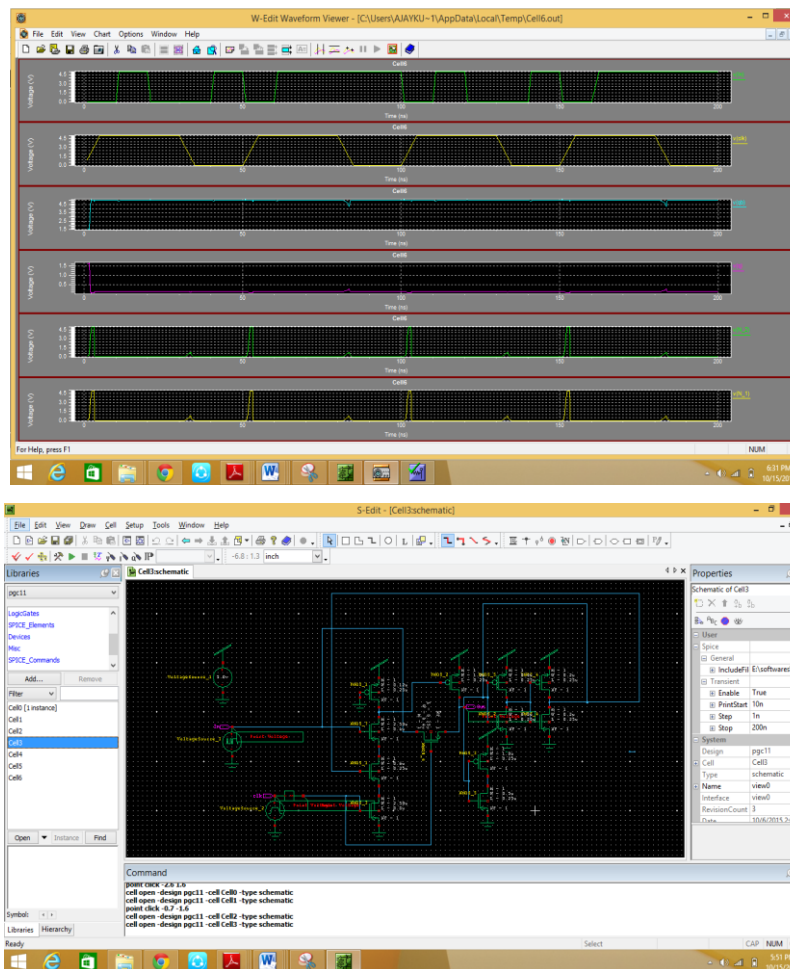
The input boosting seems to be burden to the input source but it might not be the burden since it will be active only for very short period of time. The data transition from 1to0 which makes node charged to turn off MP2 transistor. This output has to be discharged through the MNx transistor. The Mnx transistor has to be turned on for to discharge it. This will be conducting a very short period of time which can't impact the design.

The double edge triggered flip flop using signal feed through scheme is also proposed in this paper. This design will having two static latch implementation with one single pulse generation circuit. To make efficient utilization of area we have connected two modified flip flops which are connected in way such that one is working rising edge and second in enabling with falling edge such that writing speed will be high for this type of circuits.

IV. SIMULATION RESULTS

In this paper we have studied various existed designs in the literature and their drawbacks, we have proposed a solution the longer discharging problem of output node is signal feed through scheme. We have drawn all existing and proposed circuits and simulated using tanner EDA tools with TSMC25nm file. We found the proposed circuit having less power consumption and reduced delay the CDFD and SDFD. The simulated wave forms of the flip flops are as shown in below diagrams





V. CONCLUSION



The signal feed through scheme which improves delay and the Mn_x transistors which reduces the extra area needed by the inverter keeper logic, pull down network such that power needed extra circuit can be effectively reduced. The MN_x transistor will be turning only for short period of time of pulse signal that will not impact in the total circuit power. The proposed circuits and existed circuits are designed in tanner EDA tools. The simulated results will show that they need very less power as compared with ep-dco and MHL FF, having good speed with compared to the CDFE and SDFE.

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