International Journal of Innovative Research in Science and Engineering
Vol. No.3, Issue 01, January 2017
www.ijirse.com
ISSN (O) 2454-966
ISSN (P) 2454-066

PHYSICAL DESIGN, IMPLEMENTATION AND FFT ANALYSIS OF 16 BITS CARRY LOOK AHEAD ADDER CIRCUITS USING C5 PROCESS FOR DEEP SUBMICRON CMOS

Ayoush Johari[1], Aparna Gupta[2], Dr. Rita Jain[3]

[1,2] Assistant Professor, [3]Professor , Department of Electronics and Communication Engineering
Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, (India)

ABSTRACT

A full custom logic design for adders and their timing analysis followed by Fast Frequency Transform (FFT) plots is proposed in this paper targeting high speed applications using Metal Oxide Semiconductor Implementation Service (MOSIS) C5 process for Complementary Metal Oxide Semiconductor (CMOS). The characteristic of this logic style regardless of the logic type makes it suitable for implementing complicated arithmetic and logic circuits preferably adders and multipliers. A Carry-Look Ahead (CLA) Adder or fast adder is a type of adder used in digital logic and is presented for design and analysis. A carry-look ahead adder improves speed by reducing the amount of time required to determine carry bits. It can be contrasted with the simpler, but usually slower, ripple carry adder for which the carry bit is calculated alongside the sum bit, and each bit must wait until the previous carry has been calculated to begin calculating its own result and carry bits. The carry-look ahead adder calculates one or more carry bits before the sum, which reduces the wait time to calculate the result of the larger value bits. Carry Propagator and Carry Generator FFT results are compared in terms of their amplitude, phase and group delays. Several design considerations including timing window width adjustment and output distribution namely sum are discussed. Sum outputs are tabulated for multibit adders namely 4 bits and 16 bits. Their timing analysis is done using suitable SPICE code and C5 process technology.

Keywords : CMOS, Adders, VLSI Design, CAD, Process Technology, delay analysis

I. INTRODUCTION

In this paper, a full adder design employing both Complementary Metal–Oxide–Semiconductor (CMOS) logic and transmission gate logic is reported. The design was reviewed firstly implemented for 1 bit and then extended for 32 bit also. The circuit was implemented using many professional VLSI CAD tools such as Cadence Virtuoso tools in 180 and 90 nm technology. Performance parameters such as power, delay, and layout area were compared with the existing designs such as complementary pass-transistor logic, transmission gate adder,

ISSN (O) 2454-966
ISSN (P) 2454-066

transmission function adder, hybrid pass-logic with static CMOS output drive full adder, and so on. For low power voltage supply at process technology below 180-nm technology, the average power consumption few µW less than fewer µW was found to be extremely low with moderately low delay less than generally of the order of pico-seconds resulting from the deliberate incorporation of very weak CMOS inverters coupled with strong transmission gates. Corresponding values of the same were of the order of the deep submicron and µW. The design was further extended for implementing 32-bit full adder also, and was found to be working efficiently with only variable and constant delay logic styles and power tabulated at 180-nm and 90-nm and MOSIS C5 models for scalable CMOS transistors below the mentioned technology for 1.8-V or 1.2-V supply voltage. In comparison with the existing full adder designs, the present implementations were found to offer significant improvement in terms of power and speed and overall performance as well.

With the advent of Very Large Scale Integration (VLSI) and Ultra Large Scale Integration (ULSI) after that, rapid advances took place in circuit integration technologies; the electronics industry has achieved a phenomenal growth over the last two decades. Various applications of VLSI CMOS circuits in high-performance computing, telecommunications and consumer electronics has been expanding progressively and at a very hasty pace. Steady advances in semi-conductor technology and in the integration level of Integrated Circuits (ICs) have enhanced many features, increased the performance, improved reliability of electronic equipment and at the same time reduce the cost, power consumption and the system size. With the increase in the size and the complexity of the analog and digital systems, Computer Aided Design (CAD) tools are introduced into the hardware design process. Design Methodologies are necessary for a systematic design. [1, 8] The chip design process enforced the automation of process, automation of simulation based verification i.e. replacing of traditional breadboard techniques through Hardware Description Language (HDL) development. The various modular hierarchical techniques of design created the scenario that CAD tools are inevitable.

II. VLSI TECHNOLOGY AND DESIGN

A VLSI System integrates millions and millions of electronic components in a small area. The main objective is to make the analog or digital system as compact as possible with the required functionalities. Tens and thousands of transistors are fabricated on a small piece of wafer. The circuits are tested and fabricated because once an error is created the whole design is waste and it costs million and millions of dollars. Therefore CAD tools came into the picture. CAD tools are inevitable. [9] This chip design forced automation of process, automation of simulation based verification. This CAD assistance has lead to Electronic Design Automation which may be further classified in to frontend and backend design.

ISSN (O) 2454-966
ISSN (P) 2454-066

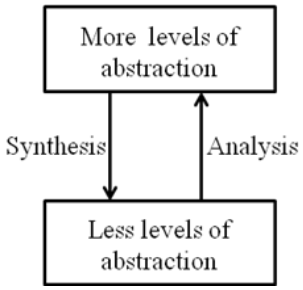

Figure 1 Abstraction Hierarchy for VLSI Adders 1

Our design methods usually differ by the number of abstraction levels and the complexities involved.

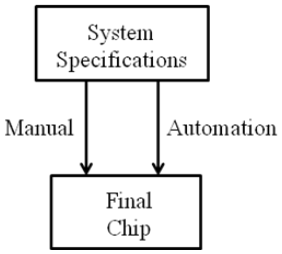

Figure 2 Abstraction Hierarchy of VLSI Adders 2

Comparing structurally different views of a VLSI Design include divide and conquer techniques which includes sorting by structure and sorting by issues. The design hierarchy that uses existing techniques has an unacceptable restriction that they use identical hierarchies. Structurally hierarchy transformation is the first step and hierarchy base comparison is the last step.

A. Structured Design Techniques
B. Programmable Logic Design
C. Gate Array and Sea of Gates Design
D. Cell Based Design
E. Full Custom and Semi custom Design
F. Platform based Design and SOC

III ADDER DESIGN METHODOLOGY

Digital design is an amazing and very broad field. The applications of digital design are present in our daily life, including Computers, calculators, video cameras etc. In fact, there will be always need for high speed and low power digital products which makes digital design a future growing business. Adders are critical component of a microprocessor and are the core component of central processing unit. Furthermore, it is the heart of the instruction execution portion of every computer. Adders comprise the combinational logic that implements logic operations, such as AND and OR, and arithmetic operations, such as ADD and SUBTRACT.

International Journal of Innovative Research in Science and Engineering
Vol. No.3, Issue 01, January 2017
www.ijirse.com
ISSN (O) 2454-966
ISSN (P) 2454-066

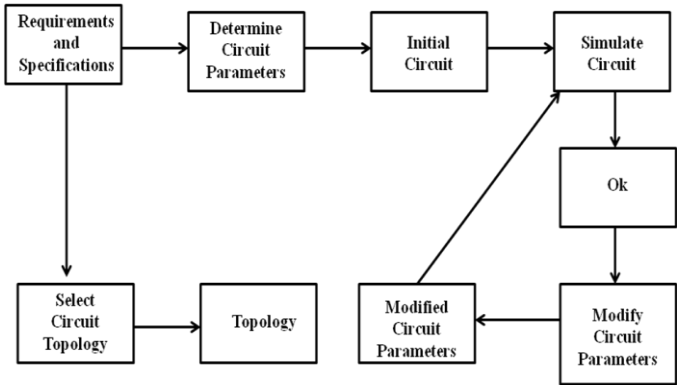

Figure 3 Present Methodology and Planning for Adder Circuit design

Methodology and Planning of Work designing of 16 bit adders is presented in figure 3 :

The design methodology can be clear from following

1. Defining the requirements and setting the specifications.
2. Design according to the tool flow (EDA based).
3. Design of the test circuits.

4. Simulating the test results and optimization of the parameters

The design methodology can be summarized as

1. Choosing the basic structure of the Adders.
2. Selection of the computational model using appropriate process technology.
3. Measurement and Optimization of Design parameters
4. Physical model implementation of the design.

IV SIMULATION RESULTS AND EXPERIMENTAL DATA

A regrious effort has been to implement the presented design. The presented design isa full custom integrated circuit design with all design rules and network consistency checks verified. The project aims to design the combinational circuits and simulate the designed circuits. The designed schematic views and icon views along with the simulation results are shown one by one along with one final integrated design. An NCC (Network Consistency Check) report is attached for the complete design.

There are numerous topologies and designs exist in literature. This paper presents a full custom design of multi bit adders starting from design of a single bit adder as shown in figure 4 and simulation results are as shown

International Journal of Innovative Research in Science and Engineering
Vol. No.3, Issue 01, January 2017
www.ijirse.com
ISSN (O) 2454-966
ISSN (P) 2454-066

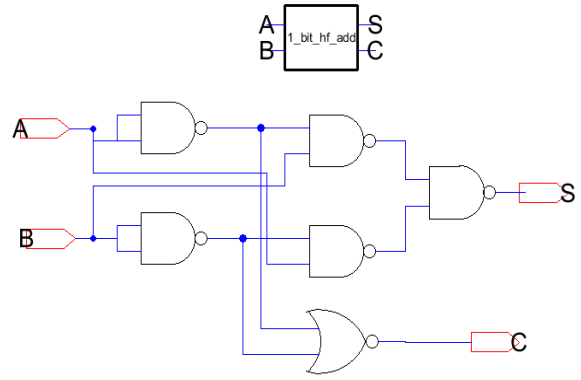

Figure 4 Schematic and icon view of 1 bit half adder

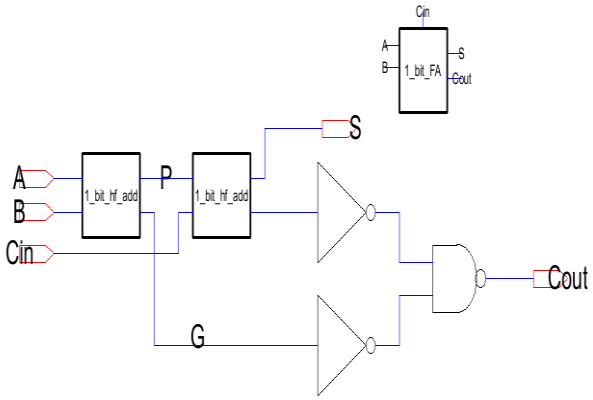

Figure 5 Schematic and icon view of 1 bit Full adder

Schematic for 1 bit full adder is shown above in figure 5 which is obtained by combining 2 single bit half adders.

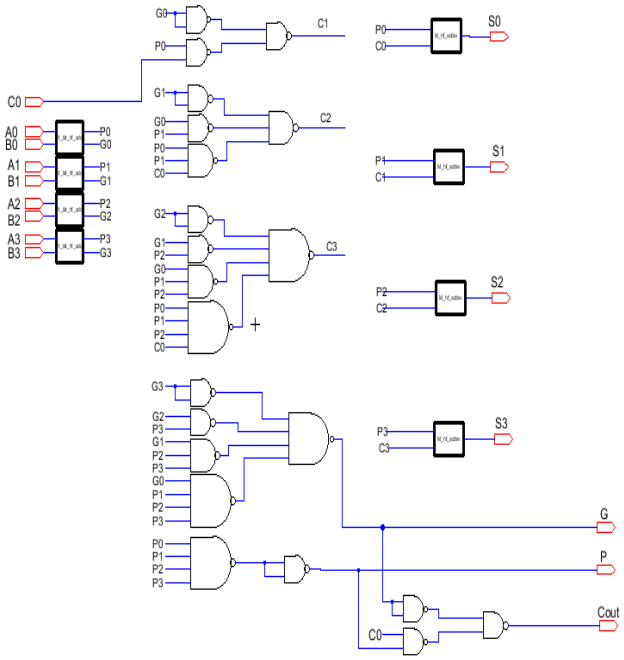

Figure 6 Schematic Design for 4 bit CLA Adder

International Journal of Innovative Research in Science and Engineering
Vol. No.3, Issue 01, January 2017
www.ijirse.com
ISSN (O) 2454-966
ISSN (P) 2454-066

In figure 6, a 4 bit carry look-ahead adder is represented. Input signals are represented by A0, B0, A1, B1, A2, B2, A3, B3, and output signals are propagate and carry signals P0, G0, P1, G1, P2, G2, P3 and G3. Further schematic includes carry signals C0, C1, C2 and C3. Further outputs include sum signals S0, S1, S2, S3 and final P, G and Cout signals.

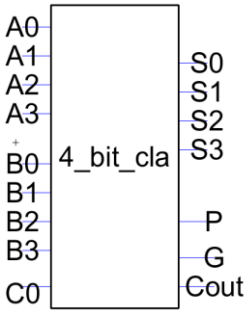

Figure 7 Icon for design for 4 bit CAL Adder with Inputs A_{0-3} and B_{0-3} and Sum Outputs Propagate, Generate and Carry out with Sum S_{0-3}

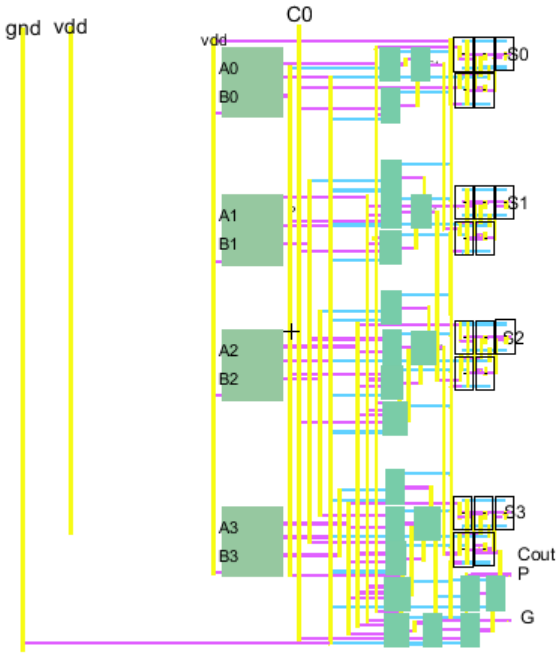

Figure 8 Physical Layout Design for 4 bit CLA Adder

Physical Design or the layout of a 4 bit carry look ahead adder is represented. Input signals are represented by A0, B0, A1, B1, A2, B2, A3, B3 and output signals are propagate and carry signals P0, G0, P1, G1, P2, G2, P3 and G3.

International Journal of Innovative Research in Science and Engineering
Vol. No.3, Issue 01, January 2017
www.ijirse.com
ISSN (O) 2454-966
ISSN (P) 2454-066

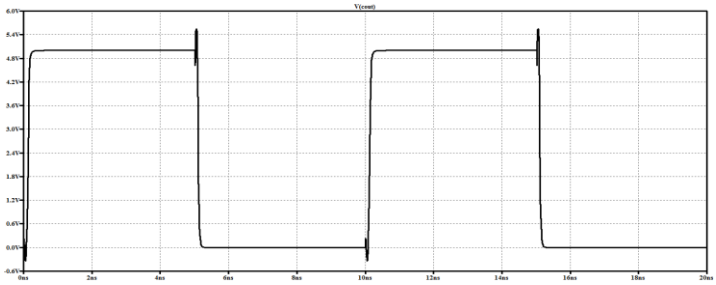

Figure 9 Transient Analysis Plot for Carry out for 4 bit CLA for 20ns

Voltage of Cout is plotted with respect to time where Y axis is in volts and x axis in seconds. The timing analysis was carried out for 20ns.

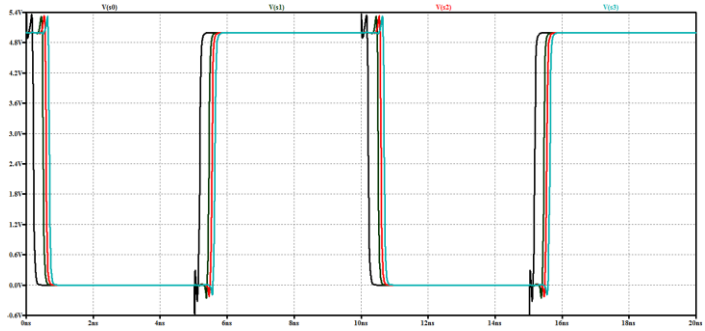

Figure 10 Transient plot for Sum signals in 4 bit CLA

In figure 10 four different voltage sum signals are plotted where y axis in volts and x axis is in seconds. All the four sum signals v(S1), v(S2), v(S3) and v(S4) were simulated for 20ns.

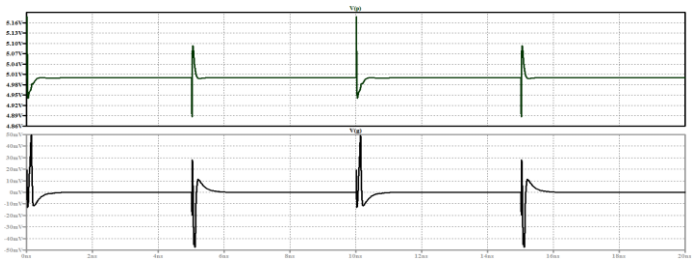

Figure 11 Transient Plot for Propagate and Generate Signals in 4 bit CLA Adder

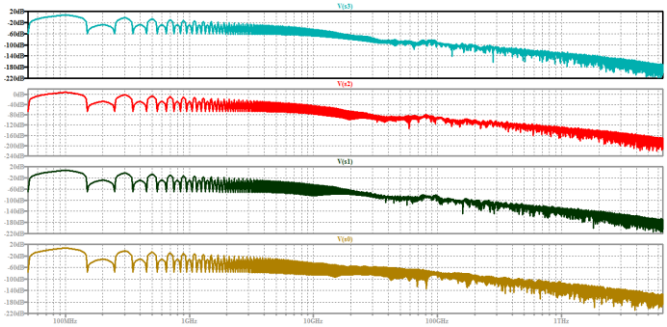

Figure 12 FFT Plots for Sum Signals in 4 bit CLA

ISSN (O) 2454-966
ISSN (P) 2454-066

FFT plots indicate noise profile for a analog and digital circuits. Above plots are obtained from transients obtained in the previous figure 10.

A 4 bit CLA icon view along with SPICE simulation script is presented. Vdd used for simulation is 5 volts. $A_{0\text{-}3}$ and $B_{0\text{-}3}$ are respectively connected to VDD and ground. Ouputs are obtained at Sum $S_{0\text{-}3}$, propagate P, generate G and carry output $C_{out.}$ Default C5 CMOS models are included for SPICE simulation

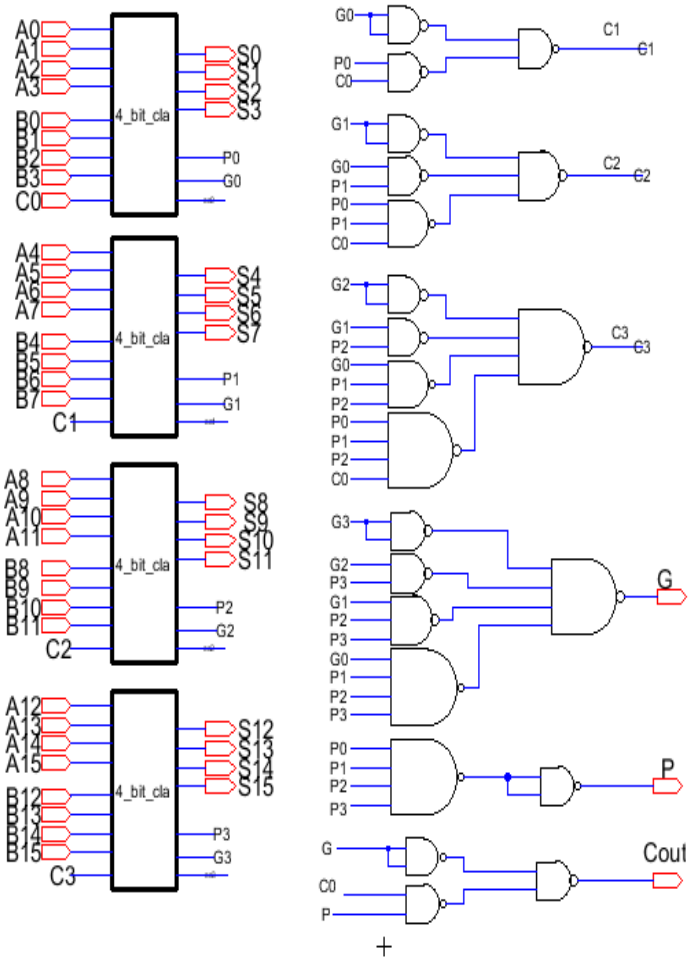

Figure 13 Schematic for 16 bit CLA Adder

In figure 13, a 4 bit CLA Adder is represented. Input signals are represented by A0, B0, A1, B1, A2, B2, A3, B3, A4, B4 A5, B5, A6, B6, A7, B7, A8, B8, A9, B9, A10, B10, A11, B11, A12, B12, A13, B13, A14, B14, A15, B15 and output signals are propagate and carry signals P0, G0, P1, G1, P2, G2, P3 and G3. Further schematic includes carry signals C0, C1, C2 and C3. Further outputs include sum signals S0, S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15 and final P, G and Cout signals.

ISSN (O) 2454-966
ISSN (P) 2454-066

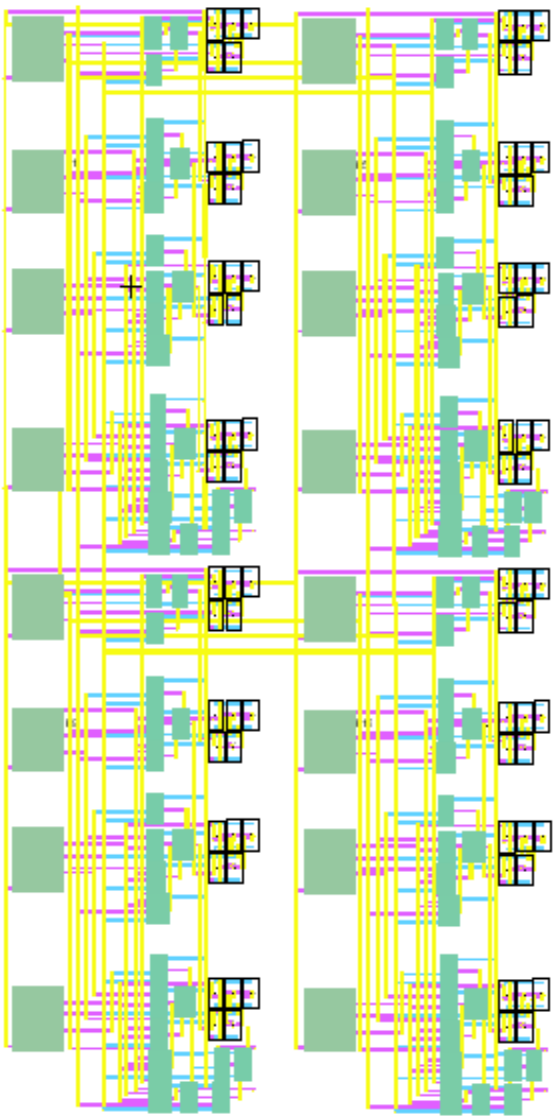

Figure14 Physical Layout of 16 bit CLA Adder

Physical Design for 16 bit design is shown in the figure 14 or the layout of a 16 bit CLA Adder is represented. Input signals are represented by A0, B0, A1, B1, A2, B2, A3, B3, A4, B4 A5, B5, A6, B6, A7, B7, A8, B8, A9, B9, A10, B10, A11, B11, A12, B12, A13, B13, A14, B14, A15, B15 and output signals are propagate and carry signals P0, G0, P1, G1, P2, G2, P3 and G3. Further schematic includes carry signals C0, C1, C2 and C3. Further outputs include sum signals S0, S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12, S13, S14, S15 and final P, G and Cout signals. Design Rule Check (DRC) and Network Consistency Checks (NCC) are satisfied for the above design, of 16 bits Carry Look Ahead Adder Circuits Using C5 Process for deep submicron CMOS which has 6 metal layers.

International Journal of Innovative Research in Science and Engineering
Vol. No.3, Issue 01, January 2017
www.ijirse.com
ISSN (O) 2454-966
ISSN (P) 2454-066

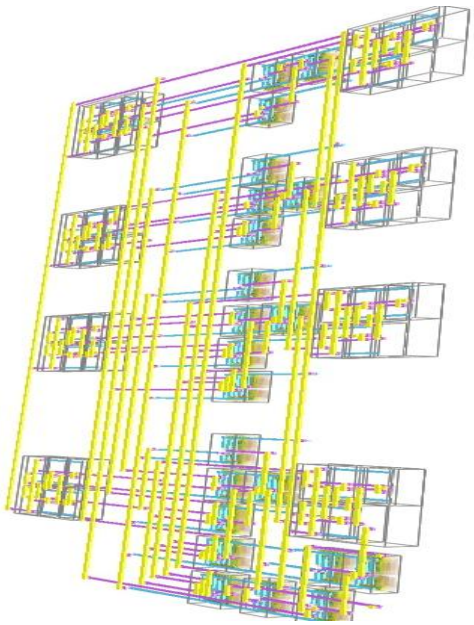

Figure15 3D View Physical Layout of 16 bit CLA Adder

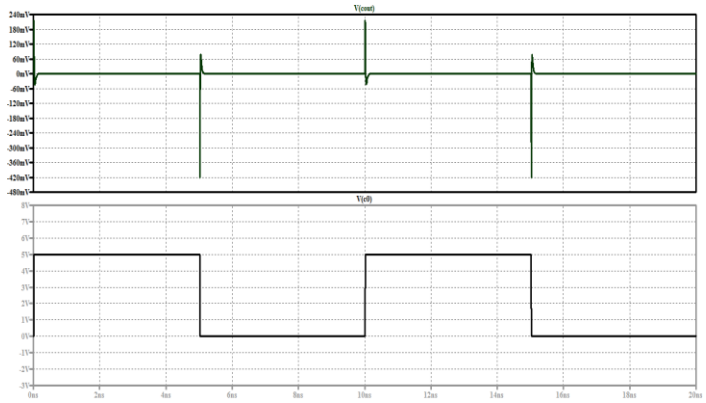

Figure 16 Transient Analysis for Carryout

Voltage of Cout and Co is plotted with respect to time where Y axis is in mill volts and volts and x axis in seconds. The timing analysis was carried out for 20ns.

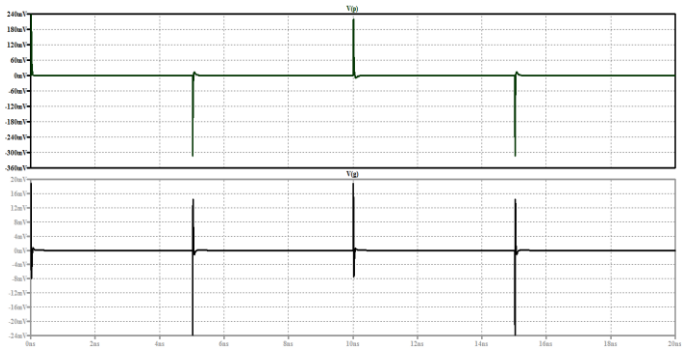

Figure 17 Transient Analysis for Propagate and Generate Signals in 16 bit CLA Adder

ISSN (O) 2454-966
ISSN (P) 2454-066

Voltage of propagate and Carry is plotted with respect to time where Y axis is in volts and x axis in seconds. The timing analysis was carried out for 20ns.

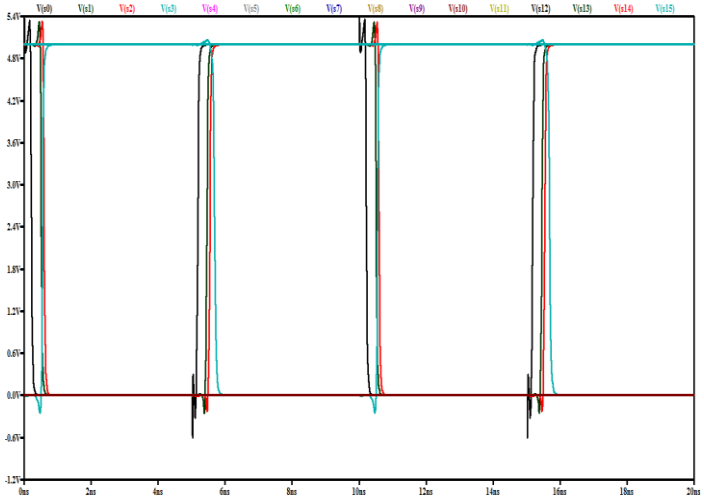

Figure 18 Transient Plot for Sum Signals in 16 bit CLA Adder

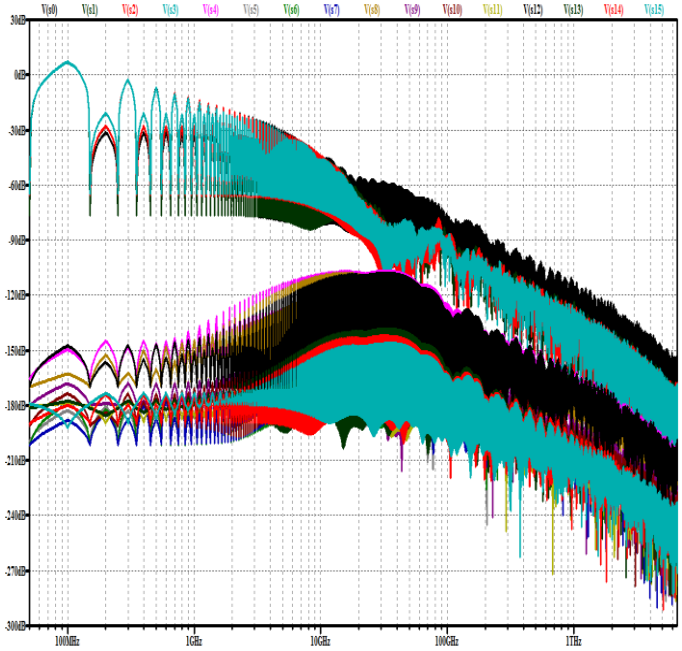

Figure 19 FFT Plots or Noise Index Plot for Sum Signals in 16 bit CLA Adder Design

FFT plots for 16 sum signals indicate noise profile for a analog and digital circuits. Above plots are obtained from transients obtained in the previous figure 18.

A 16 bit CLA icon view along with SPICE simulation script is presented. Vdd used for simulation is 5 volts. $A_{0\text{-}15}$ and $B_{0\text{-}15}$ are respectively connected to Vdd and ground. Ouputs are obtained at Sum S0-15, propagate P, generate G and carry output Cout. Default C5 CMOS models are included for SPICE simulation

ISSN (O) 2454-966
ISSN (P) 2454-066

V. FFT PLOTS COMPARISON BETWEEN 4 BIT CLA AND 16 BIT CLA

The performance analysis of adders 4 bits and 16 bits in terms of their FFT profile is shown in above and tabulation and comparison of FFT and transient parameters is illustrated here and drawn in table- 1, shows different, thus, there exist trade-off between these parameters. The results are helpful in selection of an adder according to desired result and application.

Table 1

FFT Index Results for 4 bit CLA (Sum Signals)

FFT plot parameters for signal S_0			
S.No.	**Frequency**	**Magnitude**	**Delay**
1.	10 MHz	94 dB	213 ps
	100 MHz	6 dB	49 ns
	1 GHz	94 dB	1ns
	10 GHZ	100 dB	203 ps
	100 GHz	111 dB	179 ps
FFT plot parameters for signal S_1			
2.	**Frequency**	**Magnitude**	**Delay**
	10 MHz	91 dB	522 ps
	100 MHz	6 dB	7 ns
	1 GHz	91 dB	486 ps
	10 GHZ	102 dB	551 ps
	100 GHz	115 dB	567 ps
FFT plot parameters for signal S_2			
3.	**Frequency**	**Magnitude**	**Delay**
	10 MHz	86 dB	603 ps
	100 MHz	6 dB	49 ns
	1 GHz	86 dB	2 ns
	10 GHZ	96 dB	570 ps
	100 GHz	12 dB	116 ps
FFT plot parameters for signal S_3			
4.	**Frequency**	**Magnitude**	**Delay**
	10 MHz	81 dB	698 ps
	100 MHz	6 dB	49 ns
	1 GHz	81dB	3 ns
	10 GHZ	88 dB	677 ps
	100 GHz	109 dB	808 ps

ISSN (O) 2454-966
ISSN (P) 2454-066

Table 2

FFT Index Results for 16 bit CLA (Sum Signals)

FFT Plot Parameters for Signal S_0			
S.No.	**Frequency**	**Magnitude**	**Delay**
1.	100 MHz	7 dB	4.7 ns
	1 THz	127 dB	2.55 ns
FFT Plot Parameters for Signal S_1			
2.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	6.99 dB	4.4956 ns
	1 THz	131.595dB	457.597 ps
FFT Plot Parameters for Signal S_2			
3.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	6.991 dB	4.391 ns
	1 THz	132.36 dB	2.327 ns
FFT Plot Parameters for Signal S_3			
4.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	7 dB	575.40ps
	1 THz	138 dB	1.5 ns
FFT Plot Parameters for Signal S_4			
	Frequency	**Magnitude**	**Delay**
5.	100 MHz	149dB	149.89 ps
	1THz	167 dB	1.89 ns
FFT Plot Parameters for Signal S_5			
6.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	186.8 dB	101.8 ps
	1THz	199. 9 dB	386.1 ps
FFT Plot Parameters for Signal S_6			
7.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	179.7 dB	5.5 ns
	1THz	202.4 dB	3.6 ns

ISSN (O) 2454-966
ISSN (P) 2454-066

FFT Plot Parameters for Signal S_7			
8.	**Frequency**	**Magnitude**	**Delay**
	100MHz	188.1dB	5.4 ns
	1THz	208.6 dB	153.8 ps
FFT Plot Parameters for Signal S_8			
	Frequency	**Magnitude**	**Delay**
9.	100 MHz	162.8 dB	66.4 ps
	1 THz	175.6 dB	3.8 ns
FFT Plot Parameters for Signal S_9			
10.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	168.09 dB	5.09 ns
	1 THz	196 dB	2.77 ns
FFT Plot Parameters for Signal S_{10}			
11.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	174.5 dB	4.5 ns
	1 THz	199.9 dB	4 ns
FFT Plot Parameters for Signal S_{11}			
12.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	100 dB	58 ps
	1 THz	204.5 dB	186 ps
FFT Plot Parameters for Signal S_{12}			
	Frequency	**Magnitude**	**Delay**
13.	100 MHz	147.5 dB	5. 1 ns
	1 THz	176. 6 dB	3. 7 ns
FFT Plot Parameters for Signal S_{13}			
14.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	177 dB	56 ps
	1THz	206 dB	3. 8 ns
FFT Plot Parameters for Signal S_{14}			
15.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	179cdB	5.09 ns
	1 THz	211 dB	2.73 ns

ISSN (O) 2454-966
ISSN (P) 2454-066

FFT Plot Parameters for Signal S_{15}			
16.	**Frequency**	**Magnitude**	**Delay**
	100 MHz	192 dB	75 ps
	1 THz	217 dB	1 ns

VI. CONCLUSION

With design technology, it would be possible to implement, verify and test the complex integrated circuits like adders which is the basic unit of all arithmetic circuits. This paper explains design quality metrics from an Adder design perspective, simulation and analysis of the same namely in terms of its FFT profile. Average delay for a 4 bit CLA is 30.02 ns and average delay for 16 bit CLA is 2.468 ns at 100 MHz frequency. The logic style helps to improve the overall design and delay changes by 91.77% in a 16 bit CLA over 4 bit CLA design. Various shortcomings of the current designs and methodologies to tackle the VLSI design challenges were discussed and several promising remedies and their implications on design and methodologies are explored using C5 process technology.

REFERENCES

[1] Chuang, Pierce, David Li, and Manoj Sachdev. "Constant delay logic style." IEEE Transactions on Very Large Scale Integration (VLSI) Systems 21.3 (2013): 554-565.Catherine H. Gebotys, Mohamed I. Elmasry, "VLSI Design Synthesis and Testability"

[2] Kanoriya, Lily, Aparna Gupta, and Soni Changlani. "Layout Designing and Transient Analysis of Carry Lookahead Adder Using 300nm Technology-A." (2016).

[3] Kumar, Raushan, Sahadev Roy, and C. T. Bhunia. "Study of Threshold Gate And CMOS Logic Style Based Full Adder Circuits." Proc. IEEE, 3rd Int. Conference on Electronics and Communication Systems (ICECS), IEEE. 2016.

[4] Babu, Hima, P. Maria Glenny, and Anto Yohan. "Comparison of Power and Area: 2 Bit Hybrid Fulladder Design With 2 Bit Full Adder Using CMOS Technology." Imperial Journal of Interdisciplinary Research 2.4 (2016).

[5] Senthilkumaran, K., and K. R. Kashwan. "Adiabatic constant delay logic style." Innovations in Information, Embedded and Communication Systems (ICIIECS), 2015 International Conference on. IEEE, 2015.

[6] Bhattacharyya, Partha, et al. "Performance analysis of a low-power high-speed hybrid 1-bit full adder circuit." IEEE Transactions on very large scale integration (VLSI) systems 23.10 (2015): 2001-2008.

[7] Anku Bala "Layout and Design Analysis of Carry Look Ahead Adder Using 90nm Technology", Int.Journal Of Electrical & Electronics Engg. Volume 2, spl..issue1, 2015.

[8] Amuthavalli G. and Gunasundari R, "Analysis of 16-Bit Carry Look Ahead Adder – A Subthreshold Leakage PowerPerspective", ARPN Journal of Engineering and Applied Sciences Volume-10, NO. 6, April 2015.

ISSN (O) 2454-966
ISSN (P) 2454-066

[9] V. Reethika Rao, Dr. K. Ragini, "Comparative Analysis Of 32 Bit Carry Look Ahead Adder using Constant Delay Logic", International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 10, October 2014.

[10]V. Reethika Rao, Dr. K. Ragini, "Comparative Analysis Of 32 Bit Carry Look Ahead Adder using Constant Delay Logic",International Journal of Science, Engineering and Technology Research (IJSETR), Volume 3, Issue 10, October 2014.

[11]Jagannath Samanta, Mousam Halder, Bishnu Prasad De, "Performance Analysis of High Speed Low Power Carry LookAhead Adder Using Different Logic Styles", International Journal of Soft Computing and Engineering (IJSCE), Volume-2,Issue-6, Jan- 2013.

[12] R.Kathiresan, Dr. M.Thangavel, K.Rathinakumar, S.Maragadharaj, "Analysis Of Different Bit Carry Look Ahead AdderUsing Verilog Code", International Journal of Electronics and Communication Engineering & Technology(IJECET), Volume4, Issue 4, July-August, 2013.

[13] Jatinder Kumar, Parveen Kaur, "Comparative Performance Analysis of Different CMOS Adders Using 90nm and 180nm

Technology", International Journal of Advanced Research in Computer Engineering & Technology (IJARCET) Volume 2Issue 8, August 2013.

[14]Computer aids for VLSI http://www.rulabinsky.com/steve