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Boot strapped CMOS Inverter for ultra-low power applications by using cadence tool

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ABSTRACT

This paper describes a boot-strapped CMOS inverter for ultra-low power applications. The proposed design is achieved by internally boosting the gate voltage of the transistors (via the charge pumping technique), and the operating region is shifted from the sub-threshold to a higher region, enhancing performance and improving tolerance to PVT variations. Despite the proposed bootstrapped driver operates with a sub-threshold power supply it uses fewer transistors engaging in this region by utilizing two stages. The first stage is a normal driver with PMOS and NMOS transistors that are driven by the enhancing voltage circuit (stage 2) which generates voltage levels theoretically between $-V_{DD}$ for pulling up to $2V_{dd}$ for pulling down. Our analysis shows that the proposed implementation achieves reduction in average power compared to conventional designs under a supply voltage.

Keywords: *Ultra-low power(ULP), interconnect, charge pump, driver, boosting*

1.INTRODUCTION

Recently, scaling the power supply has become an effective way to reduce energy consumption in digital systems. Supply voltage less than the threshold voltage of the CMOS (complementary metal-oxide semiconductor) circuits have emerged showing the ability to meet the requirements of ultra-low power regime (ULP). This approach is called the sub-threshold logic circuit. However, since CMOS scaling reaching its limits, the issue of global and long interconnects has become an important consideration for circuits in high speed systems due to the problem of capacitance.

In this paper, the bootstrap method is proposed because of its capability to improve the driving ability without increasing the circuit power consumed. The bootstrapped CMOS inverter provides better performance and reduces leakage current by producing a voltage swing nearly of $2V_{DD}$ to $-V_{DD}$ and driving the V_{gs} (gate to source transistor voltage) of the NMOS and PMOS respectively.

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2. LITERATURE REVIEW

In 2001, B. Sklar [7], proposed that the bootstrap has been used based on a charge pump that is a type of DC-DC converter, which utilities a capacitor holder to generate a voltage higher than the power source. In 2008, J. Kil, J. Gu and C. H. Kim[3], proposed an interconnect technique for sub threshold circuits to improve global wire delay and reduce the delay variation due to process-voltage-temperature (PVT) fluctuations. By internally boosting the gate voltage of the driver transistors, operating region is shifted from sub threshold region to super-threshold region enhancing performance and improving tolerance to PVT variations. In 2012, Y. Ho, C. Chang and C. Su[2], presented a bootstrapped CMOS inverter operated with a sub threshold power supply. In addition to improving the driving ability, a large gate voltage swing from - V_{DD} to 2 V_{DD} suppresses the sub threshold leakage current. As compared with other reported works, the proposed bootstrapped inverter uses fewer transistors operated in the subthreshold region .Hence,our proposed system reduces the average power and improves tolerance to PVT variations due to the use of boosting capacitances used in the proposed circuit.

3. EXISTING SYSTEM

CONVENTIONAL CMOS INVERTER:

The CMOS inverter circuit diagram is shown below. The general CMOS inverter structure is the combination of both the PMOS & NMOS transistors where the PMOS is arranged at the top & NMOS is arranged at the bottom. The NMOS transistor is connected at the drain (D) & gate (G) terminals, a voltage supply (VDD) is connected at the source terminal of PMOS & a GND terminal is connected at the source terminal of NMOS. Input voltage (Vin) is connected to both the gate terminals of transistors & output voltage (Vout) is connected to the drain (D) terminals of the transistor. It is very significant to observe that the CMOS device does not have any resistors, so it will be more power-efficient.

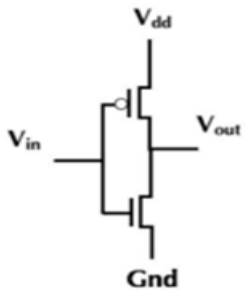

Fig 1: CMOS Inverter

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Fig 2:CMOS Inverter in schematic editor

3.PROPOSED SYSTEM

BOOTSTAPPED CMOS INVERTER:

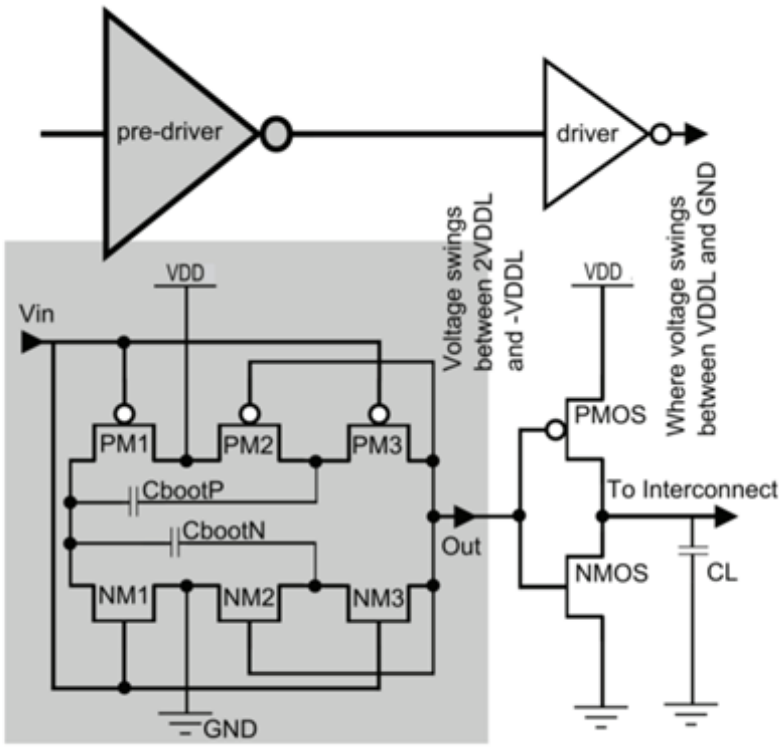

Fig 3:Bootstrapped CMOS Inverter

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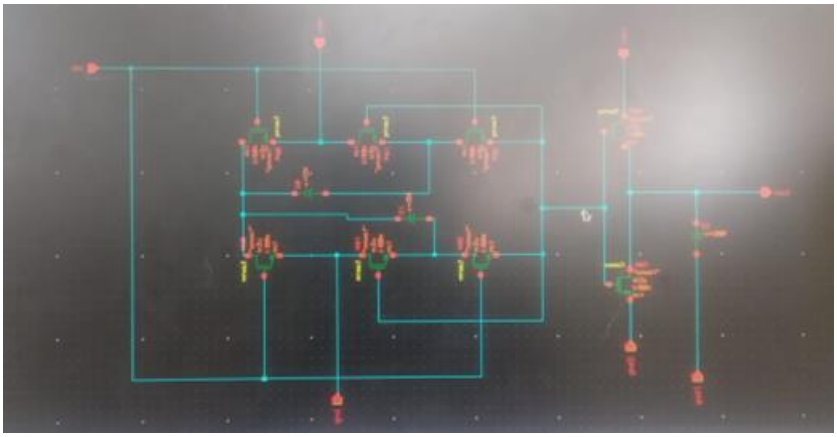

Fig 4:Boostrapped CMOS Inverter in schematic editor

In the proposed system,bootstrapped driver consists of two combinations.In general,the first one is a pre-driver that has the ability to theoretically provide a voltage swing between $-V_{dd}$ and $2V_{dd}$ to enhance the driving capability of the next stage.The next stage is a normal buffer with PMOS and NMOS transistors that are driven by the boosting voltage circuit.Figure 3 shows the circuit scheme of the proposed driver and its stages,where the pre-driver is the circuit in the middle which uses capacitors to boost the voltage.Then the buffer,which is right on the circuit,is used to drive the interconnect with a sub-threshold voltage swing from GND to $V_{dd.}$

4.METHODS OR TECHNIQUES USED IN OUR PROJECT

The Cadence tool kit consists of several programs for different applications such as schematic drawing, layout, verification, and simulation. Cadence is leading Electronic design automation (EDA) software. Cadence Virtuoso Analog Design is used for design and simulation which is the advanced design and simulation environment for the Virtuoso Platform.

5. SIMULATION RESULT

Simulation results are performed by SPECTRE in Virtuoso, Cadence at 180nm CMOS process with the 5V of input voltage and supply voltage. The proposed circuit Bootstrapped CMOS Inverter evaluated and compared to the CMOS Inverter. The power obtained of the designs are summarized in the table for 5V voltage

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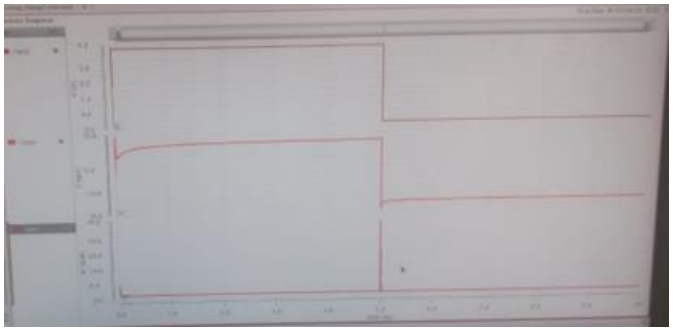

Fig 5:output waveforms of bootstrapped CMOS Inverter

Table.1: Simulation Result

S.NO	Parameter	CMOS Inverter	Bootstrapped CMOS Inverter
1.	Technology	180nm	180nm
2.	Supply Voltage	5v	5v
3.	Average Power	11.21E-6	5.852E-6

6.CONCLUSION

Interconnect drivers used in ultra-low power regime for clock distribution networks and on-chip buses suffer from considerable degradation in performance due to that fact that wire capacitance has not been scaled as the supply voltage is scaled down.Added to that, there is an issue of perfromance variability at threshold region.So,our approach has proposed using buffers with a charge pump booster, and this has met the expectations of improvements in performance by reducing power consumption.

7.FUTURE SCOPE

We have proposed a system to reduce average power by using boosting technique.It reduces the average power value compare to the existing system.In future,we will enchance the work with different types of circuits with different techniques to give the better energy savings.We can even improve the delay time performance**.**

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