International Journal of Innovative Research in Science and Engineering
Volume 08, Issue 06, 2022
www.ijirse.com
ISSN: 2454-9665

LOW VOLTAGE FREQUENCY DIVIDER WITH COMPLEMENTARY N AND P-TYPE FLIP-FLOPS

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ABSTRACT

As we have seen the vast growth in the technology, the surpassing advancements in Integrated system technologies are there is the major solid growth in using micro circuitry devices. In this digital world, electronic devices like computers, mostly use registers for multi-purposes. In this paper, a static frequency divider supported folded MOS current mode logic is presented. In an FMCML implementation, DFF is predicated on a master-slave configuration and also the schematic of one D-latch, which is the main building block. The design was implemented using 45nm Technology in Tanner EDA. It is based on alternating FMCML flip-flops with complementary pMOS or nMOS input differential pairs since common-mode problems arise by using only one type of FMCML flip-flops. In an exceedingly 2N divider, N DFFs are used, with the output of every DFF connected to the clock input of the following one. We propose a distinct approach input and output common-mode levels of every divide-by-2 block are made compatible by alternating complementary FMCML DFF stages, thus avoiding any additional stage in between. We demonstrate that the behaviour of the FMCML is different both from the one of the conventional MCML DFF and from FMCML DFF.

Keywords: *Current-mode logic, delay model, frequency divider, logic design, nanometer CMOS.*

INTRODUCTION

The mixed-signal integrated circuits that set additional requirements on the frequency divider block, in addition to a suitable frequency range for the specific application, low phase noise, and low area footprint, to ease integration, are required. Furthermore, minimization of power consumption is a fundamental issue for such systems, to enable a very high level of integration and simplify the design of packaging and heat dissipation. Among the available techniques to cope with this issue, reduction of the supply voltage can be adopted due also to the reduction of the breakdown voltage of scaled MOS devices.

The fast operation of CML circuits is mainly due to their lower output voltage swing compared to the static CMOS circuits as well as the very fast current switching taking place at the input differential pair transistors. One of the primary requirements of a current-mode logic circuit is that the current bias transistor must remain in the saturation region in order to maintain a constant current. Two frequency divider architectures in the Folded MOS Current Mode Logic which allow for operation at ultra-low voltage were analyzed and compared. The first considered architecture exploits n-Type and p-Type divide-by-two building blocks (DIV2s)

ISSN: 2454-9665

without level shifters, whereas the second one is based on the cascade of n-Type DIV2s with input level shifter. The analysis shows that the use of the forward body bias allows for designing frequency dividers that have the best efficiency. Moreover, we have found that the frequency divider architecture based on n-Type and p-Type DIV2s without a level shifter provides always better performance.

The propagation delay of the FMCML D-latch can be estimated by linearizing the circuit and applying the open circuit time-constant method. In particular, it is useful to separate the level shifter contribution from the D-latch core contribution, which is related to the bias currents.

LITERATURE REVIEW

S. Mutukuri and K. S. Pande, "Low Power Rail to Rail D Flip-Flop Using Current Mode Logic Structure," 2020 4th International Conference on Electronics, Materials Engineering & Nano-Technology (IEMENTech), 2020, pp. 1-6.

A storage element can be constructed using Current Mode Logic (CML) circuit. Folded CML D flip-flop with improved switching activity circuit suffers from static power dissipation due to always ON load PMOSFETs.

Summary: From this paper, how the average power, delay & transistor count is reduced by using Folded CML D flip-flop is studied.

Centurelli, F., Scotti, G., Trifiletti, A., & Palumbo, G. (2021). Design of Low-Voltage Power Efficient Frequency Dividers in Folded MOS Current Mode Logic. IEEE Transactions on Circuits and Systems I: Regular Papers, 68(2), 680–691.

In this paper we propose a methodology to design high-speed, power-efficient static frequency dividers based on the low-voltage Folded MOS Current Mode Logic (FMCML) approach. A modeling strategy to analyze the dependence of propagation delay and power consumption on the bias currents of the divide-by-2 (DIV2) cell is introduced.

Summary: In this paper, Folded MOS CML approach optimize the divider in maximum speed, minimum PDP.

EXISTING METHOD

MCML circuits contains true differential operation by which provides the feature of low noise level generation and static power dissipation. So the amount of current drawn from the power supply does not depends on the switching activity. Due to this MOS current mode logic (MCML) circuits have been useful for developing analog and mixed signal IC's. The implementing of MCML Dflip flop and Frequency divider done by using MCML D-latches. The proposed MCML D-latch consumes less power as it makes use of low power tri-state buffers. Which promotes power saving due to reduction in the overall current flow in the proposed D flip flop topology.

MCML Based D Flip-Flop:

Flip flops are the basic tools to store digital data. One bit of information can be stored in one flipflop. It is also utilized as data processor and memory storage elements. There is an input D (data), input clock and outputs

International Journal of Innovative Research in Science and Engineering
Volume 08, Issue 06, 2022
www.ijirse.com
ISSN: 2454-9665

called Q and Q, (inverse of Q) in basic D flip-flop. According to the input, there will be change in output. The point to be noted is that, these changes is controlled by clock signal.

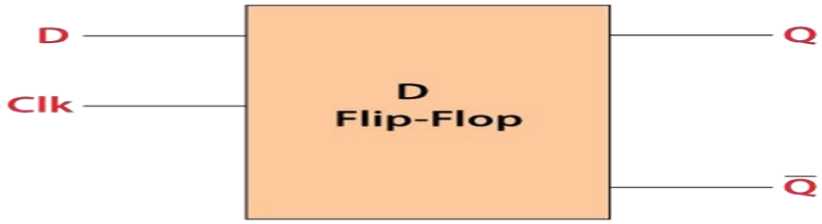

Fig.1: Basic D - flip flop.

Table.1: Truth table of D Flip flop

Clock	D	Q	Q'	Description
↓ » 0	X	Q	Q'	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1

The structure of the MCML D flip-flop is shown above. The most common approach for constructing D flip-flop is to use a master-slave configuration. The MCML D flip-flop is realized by cascading a negative latch (master stage) with a positive one (slave stage). When it is activated by the clock signal, it keeps track of the input data and transforms it to the outputs. This is known as the sampling mode of the latch.

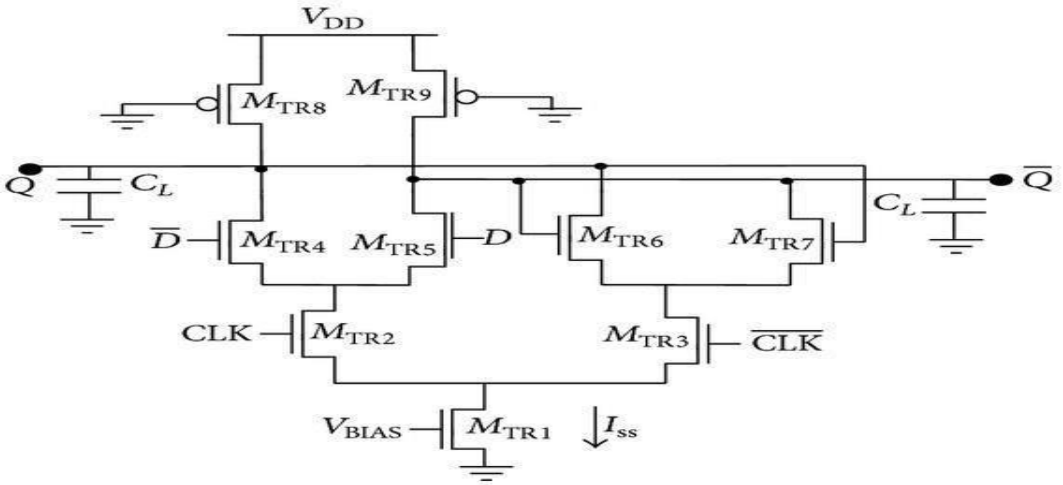

Fig.2: MCML based D Flip flop

PROPOSED METHOD

We propose a different approach input and output common-mode levels of each divide-by-2 (DIV2) block are made compatible by alternating complementary FMCML DFF stages, thus avoiding any additional stage in between. In fact, by considering the dual of the Dlatch, designed using complementary devices. In an FMCML implementation, DFF is based on a master-slave configuration and the schematic of a single D-latch, which is the main building block. In a 2N divider, N DFFs are used, with the output of each DFF connected to the clock

input of the next one. This requires the not feasible interconnection between the output of an nMOS differential pair and the input of a pMOS differential pair.

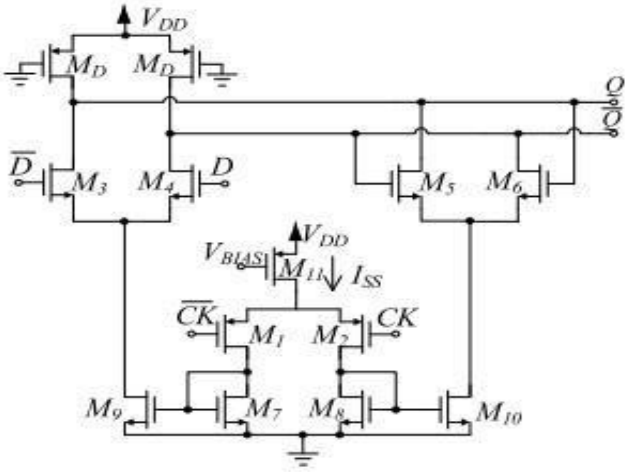

Fig.3: FMCML D-Latch

In the following, we will refer with n-type (p-type) to the DFF with the output given by an nMOS (pMOS) differential pair. The schematics of the n-type and p-type FMCML DFFs are reported in Fig. 3(a) and (b), respectively. By using these building blocks, we can realize a 2N generic static frequency divider combining them for the example of a frequency divider by 16 is shown below.

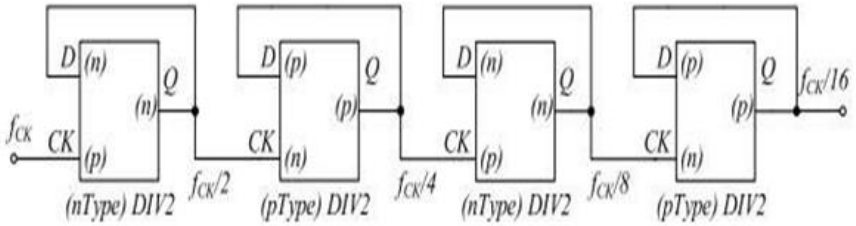

Fig.4: Proposed Frequency divider architecture

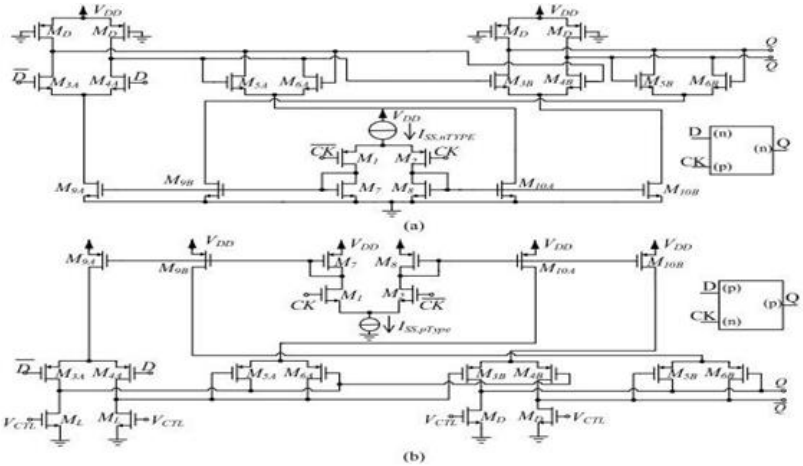

Fig.5: Topology of a) n-type b) p-type D flip flop in Folded MCML logic style.

From this, it shows that the bias currents depend on the input capacitances, including all the effects independent of the DFF bias current, ISS, nType, and depend on the ratio of the bias currents of the loading and driving

ISSN: 2454-9665

DIV2 stages, which are of the complementary type. By exchanging n-type and p-type, the same equations are valid for the CK-to-Q delay of the p-type DIV2 stage loaded by an n-type DIV2.

METHODS OR TECHNIQUES USED

The tool used for simulation purpose for the entire research work is Tanner EDA tool version 13.0. The role of EDA tool is to help design and verify a circuit's operation by numerically solving the differential equations describing the circuit. These simulation results allow circuit designers to verify and fine-tune designs before submitting them for fabrication. Tanner EDA tool is a complete circuit design and analysis system that includes:

- Schematic Editor (S-Edit): Schematic editor is a powerful design capture and analysis package that can generate netlist directly usable in T-Spice simulations.
- T-Spice Circuit Simulator: T-Spice performs fast and accurate simulation of analog and mixed analog/digital circuits.
- Waveform Editor (W-Edit): W-Edit displays T-Spice simulation output waveforms as they are being generated during simulation-Edit is a waveform viewer that provides ease of use, power, and speed in a flexible environment designed for graphical data presentation.
- Layout Editor (L-Edit): Tanner EDA tool includes L-Edit for layout editing .

RESULT

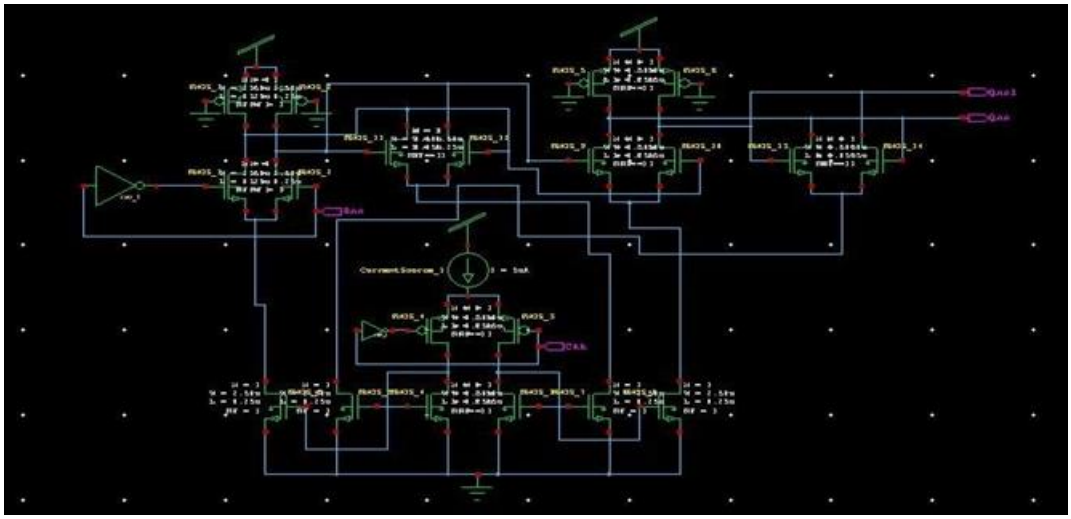

Fig.6: Schematic of n-type flip flop

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ISSN: 2454-9665

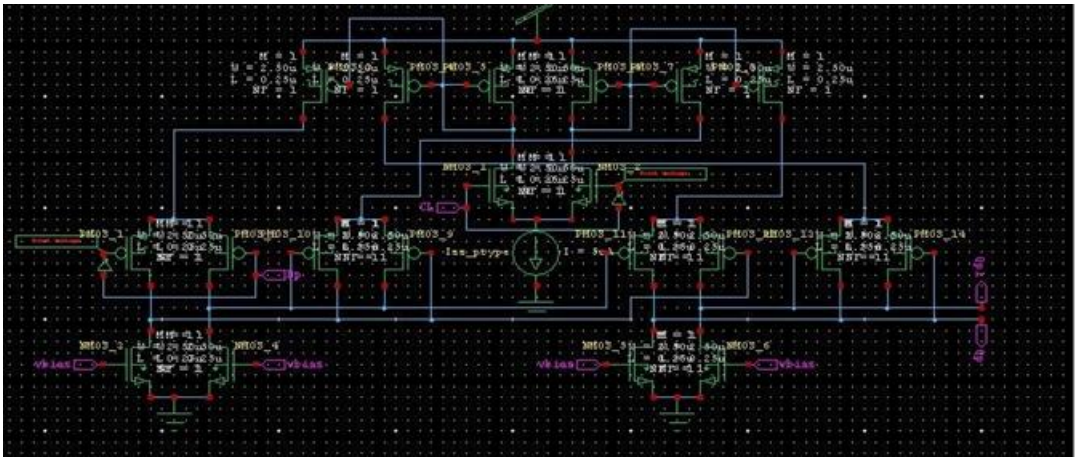

Fig.7: Schematic of p-type flip flop

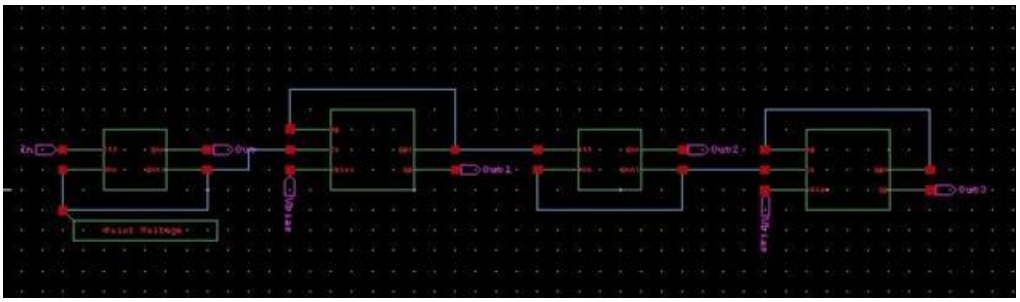

Fig.8: Schematic of proposed frequency divider in FMCML

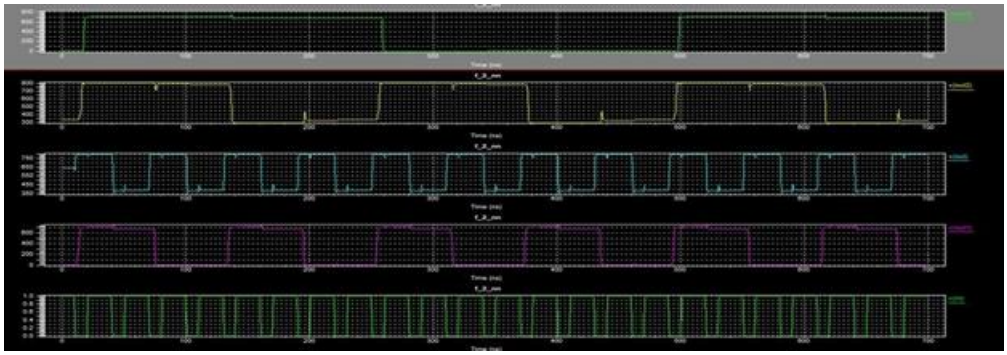

Fig.9: Output of proposed frequency divider in FMCML

ADVANTAGES

1. Minimum Power dissipation by using complementary flip flops in the design.
2. Works under the reduction of Supply Voltage.

APPLICATIONS

1. PLL-based frequency synthesizers, clock generators, and time-interleaved analog-todigital converters.

ISSN: 2454-9665

2. High speed analog/RF and digital applications require frequency dividers as key building blocks when the generation of sub harmonic signals from a high-frequency source is required.

CONCLUSION

Finally, from this paper, we concluded that a frequency divider by 16 in Folded MCML using complementary p-type and n-type flip flops is proposed. This proposed architecture is able to operate with a low supply voltage compared to MCML based architectures. As the scaling of the transistors are reducing gradually, the proposed circuit is able to work under Deep Sub-micron technology. By using complementary type of flip flops there is also a reduction of common mode problems and minimum power dissipation. In this, the control of clock is also achieved by using constant current source. By this, the propagation delay is also reduced. Due to these advantages, these are mostly used at high frequency applications, clock generators, phase locked loop circuits and radio applications.

FUTURE SCOPE

Further we can approach multi-folded (MF) MCML that generalizes the FMCML topology idea, thus allowing a minimum power supply equal to a single-level MCML (i.e., the MCML inverter) regardless of the number of inputs.

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