IMPLEMENTATION OF MULTIPLIER USING VEDIC MATHEMATICS

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ABSTRACT

Multipliers being the key components of various applications and the throughput of applications depends on Arithmetic and logic units(ALU), Digital signal processing (DSP) blocks and Multiplier and accumulate units(MAC). Vedic Multiplier has become highly popular as a faster method for computation and analysis. So that the latency of conventional multiplier can be reduced .The design of high speed Vedic multiplier that uses the techniques of Vedic mathematics based on 16 sutras (algorithms) is implemented to improve the performance. The use of Vedic Mathematics is made because it reduces the steps and time consumed in computation of partial products. In the proposed method, this process is done in a single step. The only two vedic mathematics sutras- "Urdhva Tiryagbhyam" and "Nikhilum" are used for multiplication. "Urdhva - Tiryagbhyam" is the most efficient algorithm that gives minimum delay for multiplication for all types of numbers irrespective of their size. We are going to implement the vedic multiplier using Urdhva- Tiryagbhyam Sutra on Cadence Tool. The aim is to gain high speed, less delay and hardware complexity.

I. INTRODUCTION

Multiplier is a basic building block in many processors like DSP for convolution, FFT, IDFT applications, microprocessors, MAC .In general multiplier block AND gates are used to generate partial products and adders are used to add the products. The main requirement of the processors are high speed, reduction in delay, reduction in power consumption and improved performance. It can be achieved by implementing vedic multiplier rather than conventional one .In vedic mathematics multiplier can be implemented using two sutras urdhva tiryagbhyam and nikhliam navatashcaramam. urdhava triyagbhyam means vertically crosswise and nikhliam navatashcaramam means All from 9 and the last from 10 . Commonly used sutra is urdhva triyagbhyam because it is simple, efficient and easy to understand. It can be implemented using many methods such as barrel shifter and compressors adiabatic logic.The architecture of our multiplier is based on urdhva triyagbhyam sutra.

16 Sutras of vedic mathematics:

 Ekadhikina Purvena : By one more than the previous one

 Nikhilam Navatashcaramam Dashatah : All from 9 and the last from 10

 Urdhva-Tiryagbyham: Vertically and crosswise

 Paraavartya Yojayet: Transpose and adjust

 Shunyam Saamyasamuccaye: When the sum is the same that sum is zero.

 (Anurupye) Shunyamanyat: If one is in ratio, the other is zero

 Sankalana-vyavakalanabhyam : By addition and by subtraction

 Puranapuranabyham : By the completion or non-completion

- Chalana-Kalanabyham: Differences and Similarities

- Yaavadunam : Whatever the extent of its deficiency

- Vyashtisamanstih: Part and Whole

- Shesanyankena Charamena : The remainders by the last digit

- Sopaantyadvayamantyam: The ultimate and twice the penultimate

- Ekanyunena Purvena: By one less than the previous one

- Gunitasamuchyah: The POS is equal to SOP

- Gunakasamuchyah: The factors of the sum is equal to the sum of the factors

II.LITERATURE REVIEW

In nov 2016 R.anitha et.al had implemented architecture for discrete linear convolution using vedic multiplier in cadence (45nm technology). it was noted that the design required 52% lesser area and 71.234% lesser power compared to conventional method.[19]

In may 2016 Nitesh kumar et.al had designed approximate multiplier using urdhava tiryagbhyam sutra of vedic mathematics .The design was carried out in Xilinx 14.1 . Proposed approach was divide and conquer for reducing hardware and time complexity with 20 to 30 % compared to previous one .[25]

In 2016 G.Challa ram et.al vedic multiplier is coded in Verilog HDL and is compared with design of arry multiplier in terms of delay , memory , and power comsumption.It was noticed that as we increase the no. of bits of multiplication delay can be reduced by using vedic multiplier than array multiplier.[18]

In Nov 2015 B.Keerthi priya et.al 4 bit multiplier was implemented using GDI and modified GDI technique in cadence virtuoso (45nm technology). February 6, 2017 modified GDI 75% reduction in power consumption and 53.9% reduction in delay was achieved and with the combination of carry save adder and modified GDI 80.4% and 37.6% reduction in power consumption and delay respectively.[26]

III.VEDIC SUTRA FOR   MULTIPLICATION

Urdhva Triyagbhyam :

Vedic mathematics is totally based on 16 sutras. The multiplication operation can be performed using Urdhva Tiryagbhyam" sutra (algorithm).The basic idea behind the Vedic Mathematics is to help to do almost all the numeric computations in easy and fast manner . The Sutra which we are employing in this project is Urdhva Tiryakbhyam (Multiplication).

These Sutra was anciently used for the multiplication of two numbers in the decimal number system. In this project we have applied the same idea for the multiplication of binary number system to make the algorithm that can work in digital environment . urdhva triyagbhyam means "Vertically and Crosswise". It is based on a concept in which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized by n x n bit number. The multiplier is independent of any clock frequency of processors as the partial products and their additions are calculated in parallel way.

Since it is simple structure, its layout is easily printed in microprocessors and problems can be easily known to designers and catastrophic device failures can be avoided. As it as regular structure by increasing the input and output data bus widths the processing power of multiplier can easily be increased .
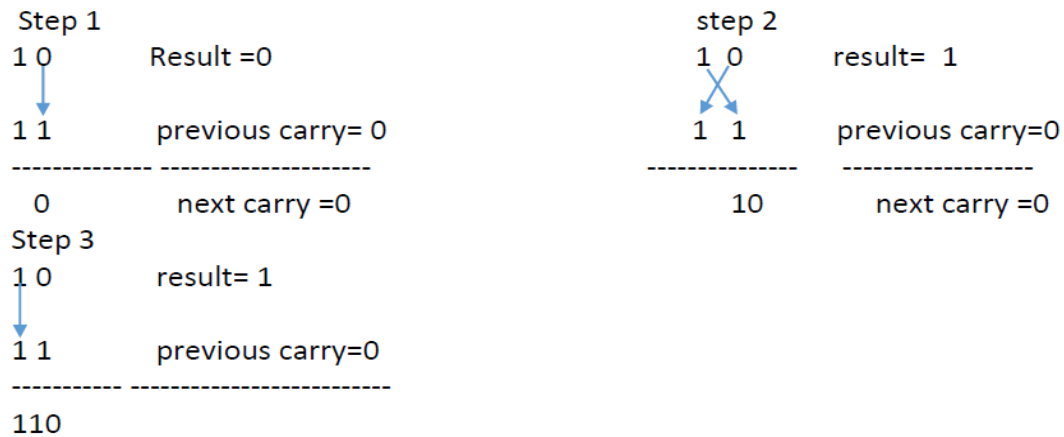
Steps for this sutra

Suppose the multiplication of two binary numbers is to be done

Consider 2x2 bit : 10 & 11

Step 1: 0 and 1 are multiplied, which becomes the LSB bit.

Step 2: The addition of (0*1) and (1*1) is performed. The LSB of this addition is placed to the left of 1 and the MSB is carry forwarded to the next stage.

Step 3: Now the multiplication of 1 and 1 is performed and the carry is added to this term.

```
Step 1                                        step 2
1 0          Result =0                         1 0          result=  1
 |
 v
1 1          previous carry= 0                 1 1          previous carry=0
-------------- ---------------------           --------------- --------------------
   0              next carry =0                    10             next carry =0
Step 3
1 0          result= 1
 |
 v
1 1          previous carry=0
----------- --------------------------
110
```

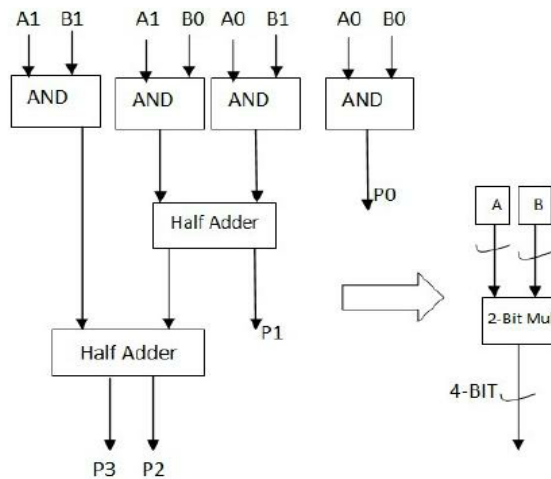## IV. 2 BIT VEDIC MULTIPLIER

fig4.1 Block Diagram

2 bit vedic multiplier is designed using two half adders as shown in figure.4.1.

Consider 2 bit inputs A(A0 A1) B(B0 B1) output is of 4 bit P (P0 P1 P2 P3)

P0=A0&B0

P1=(A0&B0)^(A1&B0)

P2=(A1&B1)^((A0&B1)&(A1&B0))
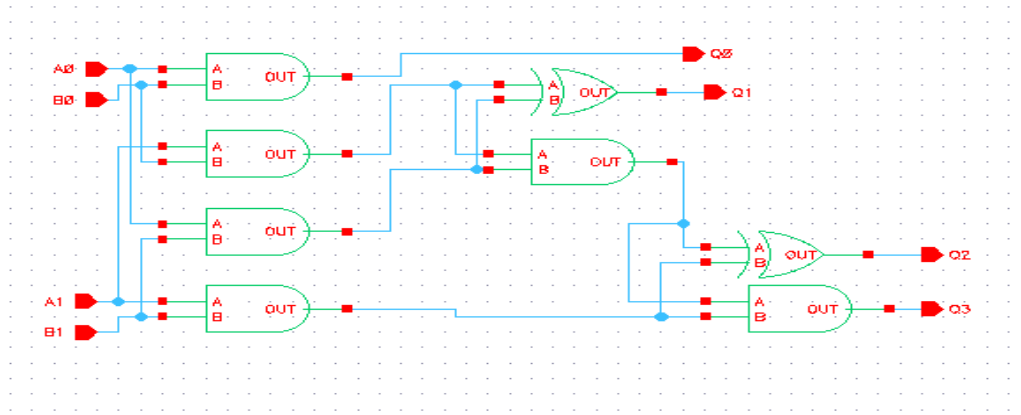
P3=(A1&B1)&((A0&B1)&(A1&B0))

V. DESIGN AND IMPLEMENTATION

 i.2x2 bit vedic multiplier

fig.5.1 shows the gate level representation of 2x2 bit vedic multiplier. It consist of 4 AND gates and 2 half adders. 2X2 bit multiplier was simulated to get the required output as shown in fig.5.2

GATE LEVEL REPRESENTATION :

SIMULATION RESULTS: IN TECHNOLOGY(90nm):

VI. GDI TECHNOLOGY

GATE DIFFUSION INPUT LOGIC,Implementation of complex logic functions are possible using only 2 transistors. GDI technique is based on use of basic simple cell as shown in fig.6
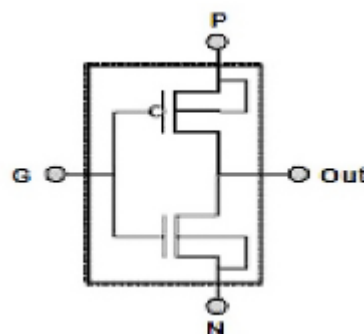

fig.6.1 GDI basic cell

GDI cell consist of 3 inputs G(common gate input of nMOS and pMOS) , P(input to the source/drain of pMOS), N(input to the source/drain of nMOS).GDI technique is suitable for design of efficient and low power circuits.it uses reduced no. Of transistors as compared to CMOS.

VII. SYNTHESIS RESULTS *(POWER CONSUMPTION uW)*

PARAMETERS	CONVENTIONAL	GDI
AND(180nm)	1.219	548.5
AND(90nm)	606.0	121.2
XOR(180nm)	2.697	2.596
XOR(90nm)	310.5	776.5
2x2 multiplier (180nm)	184.5	3.25
2x2 Multiplier (90nm)	3.65	1.69

VIII. CONCLUSION

The purpose of this implementation is to study existing methods used for multiplication using vedic maths techniques to gain better performance in terms of high speed, low power consumption and small area, also to identify the outcomes and shortcomings of the earlier work. It has been observed that in recent years many researchers have use UrdhvaTiryagbhyam sutra for the multiplication purpose. The survey identifies challenges that have not yet been resolved. In turn, this will help researchers in this area focus their research effort on those issues identified as bottlenecks and to eventually develop better multiplication techniques. Using GDI we get better performance in terms of reduced transistor count , low power and high speed.

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