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DESIGN AND IMPLEMENTATION OF C-TRANSFORM FOR MEMORY-LESS CROSSTALK AVOIDANCE APPLICATIONS

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ABSTRACT

One of the main problems in deep sub-micron designs of high speed buses is the propagation delay due to the crosstalk effect. To alleviate the crosstalk effect, there are several types of crosstalk avoidance codes proposed in the literature. In this paper, we develop explicit constructions of two types of memoryless crosstalk avoidance codes: 1) forbidden overlap codes (FOCs) and 2) forbidden transition codes (FTCs). Our constructions for both FOCs and FTCs have the largest set of codewords. To the best of our knowledge, this is the first explicit construction of a FOC that has the largest set of codewords. Our approach is based on the C-transform developed for routing optical packets in optical queues. We show such an approach can also be used for constructing limited-weight no adjacent transition codes.

Keywords: Bus-encoding, Crosstalk, Codewords, Submicron and systems-on-Chip.

I. INTRODUCTION

As VLSI technology has marched into the deep sub-micrometer (DSM) regime, new challenges are presented to circuit designers. As one of the key challenges, the performance of bus based interconnects has become a bottleneck to the overall system performance. In large designs [e.g., systems-on- chip (SoCs)] where long and wide global busses are used, inter-connect delays often dominate logic delays. Once negligible, crosstalk has become a major determinant of the total power consumption and delay of on-chip busses. The impact of crosstalk in on-chip busses has been studied as part of the effort to improve the power and speed characteristics of the on-chip bus interconnects.

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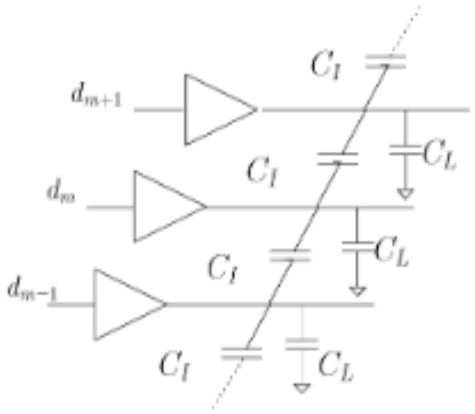

Fig. 1. On-Chip Bus Model With Crosstalk.

A simplified on-chip bus model with crosstalk denotes the load capacitance seen by the driver, which includes the receiver gate capacitance and also the parasitic wire-to-substrate parasitic capacitance is the inter-wire coupling capacitance between adjacent signal lines of the bus.

In practice, this bus structure is electrically modeled using a distributed resistance-capacitance (RC) network, after including the parasitic resistance of the wire as well (not shown in Fig. 1). For DSM processes, it is much greater than [7]. Based on the energy consumption and delay models given in [1], the energy consumption is a function of the total crosstalk over the entire bus. The delay, which deter- mines the maximum speed of the bus, is limited by the maximum crosstalk that any wire in the bus incurs. It has been shown that reducing the crosstalk can boost the bus performance significantly. Different approaches have been proposed for reducing Crosstalk by eliminating specific data transition patterns. Some schemes focus on reducing the energy consumption, while others focus on minimizing the delay. Certain schemes offer improvements in both. In this paper, we focus on crosstalk avoidance for delay reduction. As the crosstalk is dependent on the data transition patterns on the bus, patterns can be classified based on the severity of the crosstalk they impose on the bus. A more detailed explanation of pattern classification is given in Section II-A. The general idea behind techniques that improve on-chip bus speed is to remove undesirable patterns that are associated with certain classes of crosstalk. Among the proposed schemes, some are more aggressive than others (they remove more patterns and achieve higher speed improvements). Different schemes incur different area overheads since they require additional wires, spacing between wires or both. As one of the simplest techniques to eliminate the crosstalk induced delay penalty, passive shielding inserts passive (e.g., grounded) shield wires between adjacent active data lines [8]. This technique can reduce the bus delay by nearly 50%. However, it requires doubling the number of wires and hence incurs a 100% area overhead. Crosstalk can also

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be exploited to speed up the bus. Techniques such as active shielding can reduce the bus delay by up to 75% at the price of 200% or more area over- head.

II. LITERATURE SURVEY

An information theoretic framework has been developed to study the relation between speed (number of operations per time unit) and energy consumption per operation in the case of synchronous digital systems.

The theory provides us with the fundamental minimum energy per input information bit that is required to process or communicate information at a certain rate. The minimum energy is a function of the information rate, and it is, in theory, asymptotically achievable using coding. This energy-information theory combined with the bus energy model result in the derivation of the fundamental performance limits of coding for low power in deep sub-micron buses. Although linear, block linear and differential coding schemes are favorable candidates for error correction, it is shown that they only increase power consumption in buses. Their resulting power consumption is related to structural properties of their generator matrices.

In some cases the power is calculated exactly and in other cases bounds are derived. Both provide intuition about how to re-structure a given linear (block linear, etc.) code so that the energy is minimized within the set of all equivalent codes. A large class of nonlinear coding schemes is examined that leads to significant power reduction. This class contains all encoding schemes that have the form of connected Finite State Machines. The deep sub-micron bus energy model is used to evaluate their power reduction properties. Mathematical analysis of this class of coding schemes has led to the derivation of two coding optimization algorithms. Both algorithms derive efficient coding schemes taking into account statistical properties of the data and the particular structure of the bus. This coding design approach is generally applicable to any discrete channel with transition costs Coding for speed on the bus is introduced.

III. C-TRANSFORM

In this section, we first briefly review the *C*-transform and its associated properties that is developed by routing optical packets in optical queues.

Definition 1: Consider an *M*-vector $UM = (u1, u2, \ldots, uM-1, uM)$ with $ui \in \mathbf{N}$, $i = 1, 2, \ldots, M$. Define a mapping $C : x \in \{0\} \cup \mathbf{N} \rightarrow 2M$ as follows:

$$C(x) = (d1(x), d2(x), \ldots, dM-1(x), dM(x))$$

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Where $dM(x) =\_ 1$, if $x \geq uM$ 0, otherwise

and for $i = M - 1, \ldots, 2, 1,$

$di\ (x)$ is given recursively by

$di\ (x) = 1$, if $x - M\ k=i+1$

$dk\ (x) \cdot uk \geq ui$

We call C(x) the *C*-transform of *x* with respect to the basis vector *UM*. Intuitively, we can view the *C*-transform as a "greedy" binary numeral system as the *C*-transform of *x* is obtained by recursively subtracting *x* from *uM*. In particular, if we choose $ui = 2i-1$ for all *i* , then the *C*-transform of *x* is simply the usual binary representation of *x*. In addition, if we choose $ui = 2i-1 \_$, $1 \leq i \leq s$ and $ui = i-1 \quad =i-s\ u$, $i \geq s + 1$, then it is the normal-form Fibonacci number system of order *s*. One of the most important properties of the *C*-transform is the complete decomposition property, i.e., every integer (within the representation range) can be written as a sum of distinct *ui* 's. For example, consider the five-vector *U*5 = *(*1, 2, 3, 6, 10*)* as the basis vector. Then, *C(*14*)* = *(*1, 0, 1, 0, 1*)*. Note that 14 = 1×1+0×2+1×3+0×6+ 1×10 and it can be written as a sum of distinct *ui* 's. The complete decomposition property was previously proved in Lemma 5 and it is stated formally in the following proposition. A similar result was also reported in Lemma 3.1.

In this section, we show how one can construct memoryless FOCs by using the C-transform. Consider a symbol set S. An M-dimensional memoryless binary code C for S is a mapping that maps every element in S to a codeword with an M-dimensional binary representation. An M-dimensional memoryless binary code for S is a forbidden overlap code (FOC) if a transition from one codeword to another codeword does not have the following two types of transitions for any three adjacent bits: 101→010 or 010→101. Algorithm for the construction of a FOC: Symbol set: Let u1 = 1, u2 = 2, u3 = 4 and ui+1 = ui + ui−1 + ui−2 for i = 3,...,M −1. Consider the symbol set S ={0,1,2,...,uM + uM−1 + uM−2 −1}. Encoding: For x ∈ S, compute the C-transform of x, C(x) =d1(x),d2(x),...,dM−1(x),dM(x).Generate the M-dimensional binary codeword for x, denoted by c(x) = c1(x),c2(x),...,cM(x)), by ci(x) =di(x), if i is odd, 1−di(x), if i is even. Decoding: For a binary codeword c = (c1,c2,...,cM), generate the M-vector (d1,d2,...,dM) by di =ci, if i is odd, 1−ci, if i is even.

Decode the codeword c as

x = M X i=1 di ·ui. (8) Note that the steps are simply to invert every even-numbered bit. Thus, they are inverse functions of each other.

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Since we choose u1 = 1, u2 = 2, u3 = 4 and

ui+1 = ui +ui−1 +ui−2 for i = 3,...,M −1, the assumption (A1) in Proposition 2 holds and thus we have from the complete decomposition property that every codeword can be decoded correctly by using (8). In the following theorem, we show that the set of codewords generated by the above algorithm is indeed a FOC.

Theorem : The set of codewords

{c(x) =(c1(x),c2(x),...,cM(x)), x ∈ S} generated by the above algorithm is indeed a FOC. Moreover, it is optimal in the sense that it has the largest number of codewords in a memoryless M-dimensional FOC.

Proof: For this, we need to show a transition from one codeword c(x1) to another codeword c(x2) does not have the following two types of transitions for any three adjacent bits: 101→010 or 010→101. We prove this by contradiction. First, since we choose u1 = 1, u2 = 2, u3 = 4 and ui+1 = ui + ui−1 + ui−2 for i = 3,...,M−1, the assumptions (A1) and (A2) in Lemma 3 are satisfied with ` = 3. Thus,we know from Lemma 3 that for all x ∈ S, there are no three consecutive 1's in C(x).

Case 1: There is a transition of 101→010: Suppose that for some x1,x2 ∈ S and some i such that (ci(x1),ci−1(x1),ci−2(x1)) = (1,0,1) and (ci(x2),ci−1(x2),ci−2(x2)) = (0,1,0). If i is an even number, then di(x2) = 1 − ci(x2), di−1(x2) = ci−1(x2), and di−2(x2) = 1−ci−2(x2). Thus, we have (di(x2),di−1(x2),di−2(x2)) = (1,1,1). There are no three consecutive 1's in the

C-transform. On the other hand, if i is an odd number,

di(x1) = ci(x1), di−1(x1) = 1 − ci−1(x1), and di−2(x1) =ci−2(x1).

Thus, we have

(di(x1),di−1(x1),di−2(x1)) = (1,1,1).

This also contradicts to the result that there are no three consecutive 1's in the C-transform. Case 2: There is a transition of 010→101: The argument for this case is exactly the same as Case 1 with x1 and x2 being interchanged. It is known (see e.g., [12], [2]) that the largest number of codewords in a memoryless M-dimensional FOC is NM, where NM is characterized by the following recursive equation: Ni+1 = Ni + Ni−1 + Ni−2, 3≤ i ≤ M −1, N1 = 2, N2 = 4, and N3 = 7. It is easy to see from that Ni = ui+1, 1 ≤ i ≤ M − 1 and NM = uM +uM−1 +uM−2. Thus, our construction of the M-dimensional FOC indeed has the largest number of codewords.

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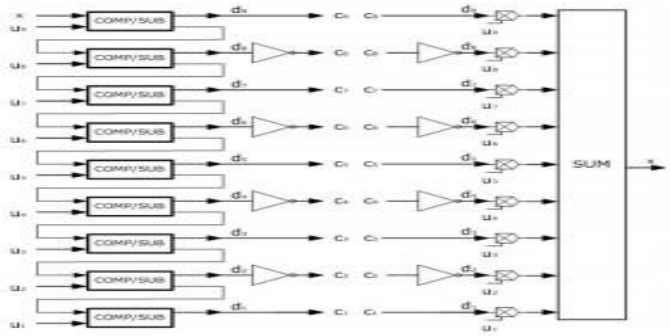

Fig. 2. 8B/9B FOC Encoder

As shown, efficient FOC codes cannot be constructed by using their numeral systems. Instead, they only construct a suboptimal FOC using their numeral systems. In comparison with the suboptimal FOC, we note that the (asymptotic) code rate is 0.7925, while the code rate of our optimal memoryless FOC is 0.8791. The key difference between theirs and ours is that we add the inverters on the even-numbered buses so that an optimal FOC can be represented by using numeral systems and these inverters. We also note that the hardware implementation complexity of our algorithm is O(M2). This is the same as those because they all require implementing numeral systems. As an illustrating example, we show the block diagram of the 8B/9B FOC encoder and decoder in Figure 1. The encoder takes an 8-bit input and encodes it into a 9-bit codeword. The basis vector (u1,...,u9) is shown in the 8B/9B FOC column of Table I. The COMP/SUB processing unit in the encoder in Figure 1 is further illustrated in Figure 2. These are similar to the implementations of the numeral systems (except the additional inverters). The decoder in Figure 1(b) takes a 9-bit codeword and decodes it into an 8-bit output. It consists of three stages. In the first stage, all the even-numbered bits are inverted. In the second stage, the ith output after the first stage is then multiplied by ui i = 1,2,...,9. In the third stage, the 8bit output is generated by summing up the outputs from the second stage. Recently, Mutyam used the transition signaling technique to construct FTCs. The transition signaling technique takes a set of input data indexed in time and computes the transition signals (by using the exclusive OR operation)

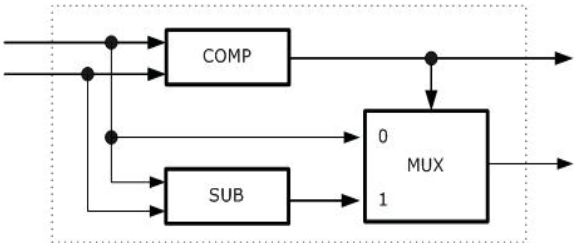

Fig. 3. COMP/SUB processing unit in the encoder.

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between any two successive input data. The transition signals are then sent through the bus. We note that the transition signaling technique can also be used here to construct FOCs. It is easy to show if there are no 3 consecutive 1's in each input data, then by sending the transition signals of these input data there are no transitions for any three adjacent bits: 101 → 010 or 010 → 101. However, the FOCs constructed this way are not memoryless as the encoder has to store the previous input data for computing the transition signals. Moreover, a simple bit error in the bus might have a cascading effect in the decoder that might cause a serious decoding failure. Since both the transition signaling technique and our construction for FOCs have the same encoding efficiency, our memoryless construction is clearly a better choice than the transition signaling technique as it not only requires lower hardware implementation complexity (in both encoding and decoding) but also it is more reliable in decoding (as it does not have the cascading decoding failure problem).

We note that our approach can also be used for the constructions of optimal memoryless FTCs. This is done by choosing the basis vector with $u1 = 1$, $u2 = 2$, and $ui+1 = ui + ui-1$ for $i = 2, \ldots, M - 1$. For the symbol set

$S = \{0, 1, 2, \ldots, uM + uM-1 - 1\}$, we can then construct an optimal FTC using the encoding scheme and the decoding scheme described in the algorithm for the construction of a FOC. Even though the construction and ours are both optimal, these two sets of codewords are different as each codeword has a Fibonacci representation. As an illustrating example, we can use the block diagram in Fig. 1 for a 6B/9B FTC encoder/decoder. The basis vector $(u1, \ldots, u9)$ is shown in the 6B/9B FTC column of Table 1.

Table 1. Basis vectors for the 8B/9B FOC, the 6B/9B FTC, and the (9, 6, 3)-NAT code.

	8B/9B FOC	6B/9B FTC	(9, 6, 3)-NAT code
U1	1	1	1
U2	2	2	2
U3	4	3	3
U4	7	5	5
U5	13	8	8
U6	24	13	12
U7	44	21	20
U8	81	34	32
U9	149	55	48

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IV. SIMULATION RESULTS

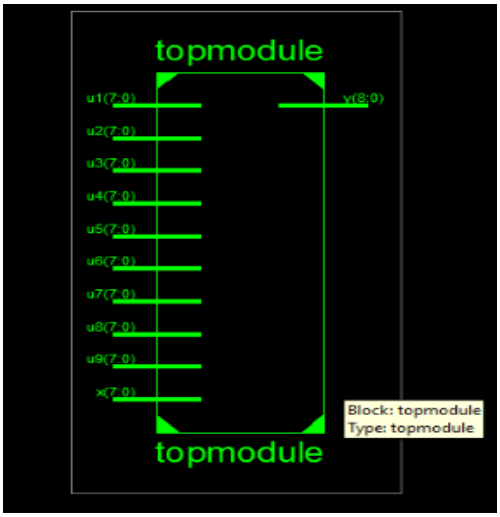

Fig. 4. RTL Schematic Diagram

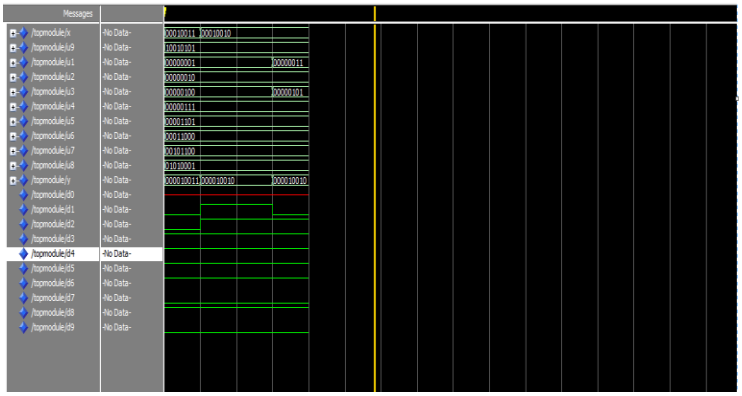

Fig. 5. Simulation Results.

topmodule Project Status (10/18/2016 - 14:58:00)			
Project File:	asasasasaea.xise	**Parser Errors:**	No Errors
Module Name:	topmodule	**Implementation State:**	Synthesized
Target Device:	xc3s50an-4tqg144	**• Errors:**	No Errors
Product Version:	ISE 14.1	**• Warnings:**	12 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	0	704	0%
Number of bonded IOBs	89	108	82%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Tue Oct 18 14:58:00 2016	0	12 Warnings (0 new)	0
Translation Report	Out of Date	Tue Oct 18 14:57:50 2016	X 2 Errors (0 new)	0	0
Map Report					
Place and Route Report					

Fig. 6. Synthesis Report.

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V. CONCLUSION

We developed an explicit construction for a set of memory-less FOCs. Such a set of memory-less FOCs also contains the largest number of codewords. The same approach can also be applied for the construction of a set of memory-less FTCs and a set of NAT codes. Both FOCs and FTCs considered in this paper are memory-less codes, and their code rates could be significantly improved by considering codes with memory. It was shown that there exists a simple bit stuffing algorithm that yields a much higher code rate than the Fibonacci representation .Besides, it hardware implementation complexity is only O(M) for an M-bit bus, which is also much lower than the O(M2) complexity. Extension along this line for FOCs will be reported separately.

REFERENCES

[1]. X. Wu and Z. Yan, "Efficient CODEC designs for crosstalk avoidance codes based on numeral systems," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 19, no. 4, pp. 548–558, Apr. 2011.

[2]. C. Duan, V. C. Calle, and S. Khatri, "Efficient on-chip crosstalk avoidance codec design," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 17, no. 4, pp. 551–560, Apr. 2009.

[3]. C. Duan, C. Zhu, and S. P. Khatri, "Forbidden transition free crosstalk avoidance CODEC design," in Proc. 45th Annu. DAC, Anaheim, CA, USA, 2008, pp. 986–991.

[4]. C.-C. Chou, C.-S. Chang, D.-S. Lee, and J. Cheng, "A necessary and sufficient condition for the construction of 2-to-1 optical FIFO multiplexers by a single crossbar switch and fiber delay lines," IEEE Trans. Inf. Theory, vol. 52, no. 10, pp. 4519–4531, Oct. 2006.

[5]. P. Subramanya, R. Manimeghalai, V. Kamakoti, and M. Mutyam, "A bus encoding technique for power and cross-talk minimization," in Proc. IEEE 17th Int. Conf. VLSI Design, Feb. 2004, pp. 443–448.

[6]. M. Mutyam, "Preventing crosstalk delay using Fibonacci representation," in Proc. 17th Int. Conf. VLSI Design, Mumbai, India, Jan. 2004, pp. 685–688.

[7]. P. P. Sotiriadis, "Interconnect modeling and optimization in deep submicron technologies," Ph.D. dissertation, Dept. Electr. Eng. Comput. Sci., Massachusetts Institute of Technology, Cambridge, MA, USA, 2002.

[8]. B. Victor and K. Keutzer, "Bus encoding to prevent crosstalk delay," in Proc. IEEE/ACM ICCAD, San Jose, CA, USA, Nov. 2001, pp. 57–63.