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SINGLE MAC IMPLEMENTATION OF A 32-COEFFICIENT FIR FILTER USING XILINX

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ABSTRACT

A major trend in the VLSI semiconductor design industry is embedded computing systems, have grown tremendously in recent years. A popular moore's law says that the integration of transistors on a single chip doubles every 18 months, which turns into their complexity. This complexity demands a new type of designer, who can cross the traditional border like complexity, delays, power utilization and to overcome drawbacks of previous designs. Due to advances in VLSI technology, programmable DSP devices are becoming necessary in the signal processing field. To achieve faster signal processing we need separate and faster processors, well known as DSP processors. To achieve implementation of high speed processors, the main processing bottlenecks are the MAC unit, digital filters, which greatly depends on the multiplier, and which greatly depends on the number of multiplication and adder units. In this paper we have proposed an improved time, less complexity design, reduced area of efficient vedic MAC unit and digital FIR filter. So we propose vedic MAC unit, compared with present conventional architectures and its application in designing digital FIR filter of 8 tap and 32 tap filter. The proposed architectures are in Verilog coding, synthesized and simulated using Xilinx ISE 9.1i

Index Terms: MAC, Multipliers, adders, FIR filter

I. INTRODUCTION

Fast execution of algorithms is our essential requirement of a digital signal processing architectures. In order to meet this requirement, DSP architecture must include features that facilitate high speed of operation, less design complexity and large throughputs. In this paper we design a multiplier starting from array, Brown, Wallace and Vedic multipliers of 2x2, 4x4 and 8x8 bits. Adders of RCA and CSA 8x8bits, number of different combination of MAC units using above multipliers and adder units and compare their design relationship. Finally we propose MAC unit application in designing of 8tap and 32tap FIR digital filter. We proposed a MAC unit consisting of adder and accumulator in a same block.

The key component of MAC unit is multiplier that multiplies two n-nit numbers X and Y and gives a product of 2n bits wide, which is added with the contents of the accumulator and saved in the accumulator. Accumulator is acts like a temporary register. Here we have designed MAC units using different combination of multipliers and adders and compare the features mainly speed and area. The speed of the MAC unit is greatly depends on the reduced delay of multiplier. Hence with the suitable choice of the type of the multiplier, the performance of the MAC unit can be made better. Hence we are proposing MAC unit consisting of adder and accumulator in a

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same block, by this delay can be decreased and other better performance can be seen in future applications like FIR filter design using MAC unit..

II. MAC OPERATION

Multiply and accumulate unit mainly used in DSP applications. It consists of mainly multiplier, adder and temporary register as an accumulator. We have designed adder and accumulator in a same block. For this model first apply inputs mxn bits to the multiplier which is being fed from the memory location.

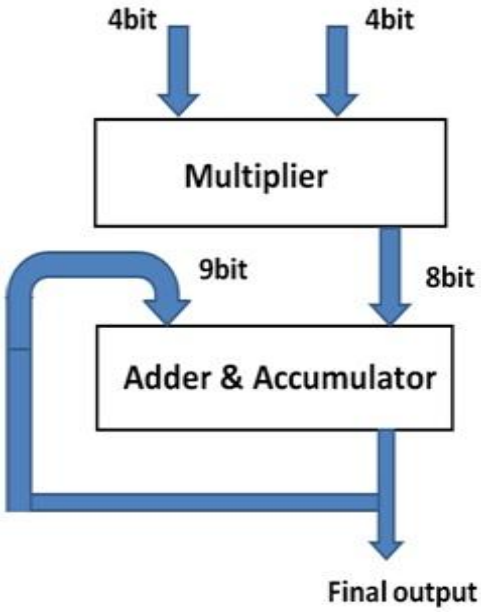

Figure 1: MAC Block diagram

The output of this will be m+n bits which are applied to adder and accumulator unit which is added with the content of the accumulator and save in the accumulator. Primarily the content of accumulator is set to zero, Which is keep on updating with clock cycles, so it is called as temporary register. The final output of accumulator will be m+n+1 bit. The block design is shown in figure in the following sections we design number of different MAC units.

III.DIFFERENT MAC UNITS

A. Vedic MAC unit of 4x4bit model

Here we use vedic multipliers of 4x4bit multiplier and simple adder for addition. The vedic multiplication uses 6bit, 4bit CSA while designing a multiplier. Here we can use RCA which is better than CSA.

B. Braun 4x4 bit MAC module

Here we use braun multiplier and simple adder for addition. Braun multiplier uses full adders. This multiplier requires 15-multiplications and 12 additions in between adjacent bits.

C. Array 4x4 bit MAC module

Here we use array multiplier followed by simple addition operation. This multiplier uses 15 multiplication and addition operations for designing..

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D. Wallace 4x4 bi MAC Module

This design unit uses Wallace multiplier followed by simple addition. Compare to other multipliers this uses 26 multiplication and 16 addition operations while designing this multiplier..

IV. APPLICATION OF MAC UNIT

Design of digital FIR filter using MAC unit as the main processing unit

We have proposed 8-tap (8 coefficients) and 32-tap (32 coefficients) FIR filter. The filter can be implemented in many ways depending on the number of multipliers and accumulators available. In this paper we have implemented using a single MAC unit.

There block diagram is shown in fig: which consists of two multiplexers and single MAC unit. The multiplexer is used to select only one input at a time which is fed to the multiplier at a given time. As each product term is generated, it is added to the previously accumulated sum in the MAC unit. Each input sample is delayed from the previous sample by 8T, where T is the time taken by the multiplier and accumulator to compute one product term and add it to the previously accumulated sum in the accumulator.

We are designing a module which implements the FIR equation

$$\text{i.e } y(n)=\sum_{i=0}^{k} h(i)\, x(k-i)$$

where k=L+M-1

L= length of x(n) signal

M= length of h(n)

E. Single MAC implementation of an 8-tap FIR filter:

Here we consider x(n) as a 8 samples and h(n) has 8 coefficients, so we used 8:1 mux of two quantities. These multiplexer selects first one sample i.e x(n) and first coefficients h(0) applies to MAC unit. A MAC unit is a single bit MAC unit. The output of this will be saved in accumulator which will be wide bits. In the next clock cycle it selects next sample x(n-1) and next coefficient h(1) and performs MAC operation on these inputs. So this will be apply for all the bits one by one and final output will be y(n) which is saved in accumulator. Here we are using the direct amplitudes of the samples and coefficients

Therefore for above equation x(n)-{11111111} h(n)={11011110}

K=8+8-1=15

We start from x(n),x(n-1)_ _ _ _ x(n-15) and h(0),h(1)_ _ _ _h(15).

F. *Single MAC implementation of an 32-tap FIR filter*

Here we consider x(n) as a 32 samples and h(n) has 32 coefficients, so we used 32:1 mux of two quantities. These multiplexer selects first one sample i.e x(n) and first coefficients h(0) applies to MAC unit. A MAC unit is a single bit MAC unit. The output of this will be saved in accumulator which will be wide bits. In the next clock cycle it selects next sample x(n-1) and next coefficient h(1) and performs MAC operation on these inputs. So this will be apply for all the bits one by one and final output will be y(n) which is saved in accumulator. Here we are using the direct amplitudes of the samples and coefficients.

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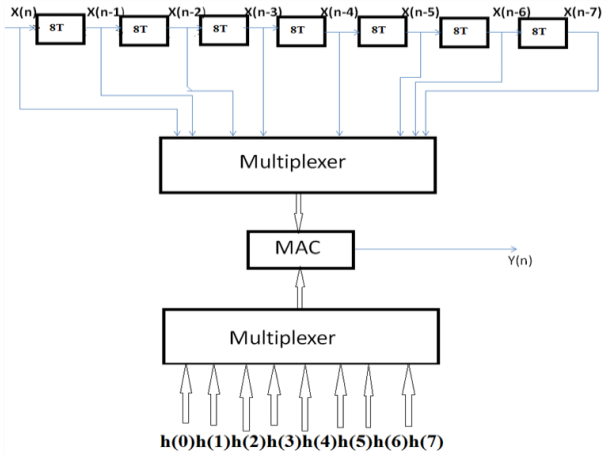

Figure 2: Single MAC implementation of an FIR filter

K=32+32-1=63

We start from x(n),x(n-1)_ _ _ _ x(n-63) and h(0),h(1)_ _ _ _h(63).

V. RESULTS

The design is done using Verilog-HDL by using tool Xilinx ISE 10.1i and target family Spartan 3E,Device-XC3S100,speed -5,package: FG320.

S.No.	MAC Unit	Logic Delay	Route Deay	Total Delay
1.	Vedic4x4 MAC Unit	20.930	4.946	25.876
2.	Braun4x4 MAC Unit	21.176	7.952	29.128
3.	Array4x4 MAC Unit	23.926	9.310	32.448
4.	Wallace 4x4 MAC Unit	21.176	8.039	29.215

TABLE I. Comparison of combinational delay with various 4x4 bit MAC units

S.No	FIR filter	Logic delay	Route delay	Total delay
1.	8-Tap	3.991ns	0.532ns	4.522ns
2.	32-Tap	5.638ns	0.532ns	6.17ns

TABLE II: Comparison of combinational delay

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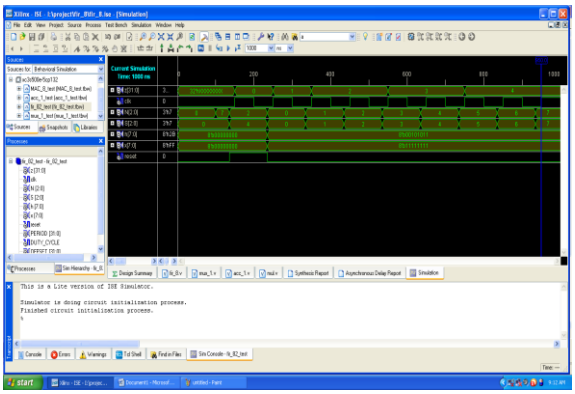

Figure 3: 8Tap FiR filter simulation Result

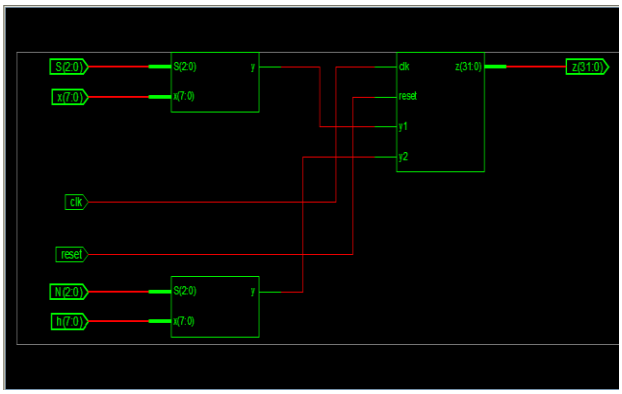

Figure 4: 8Tap FIR filter RTL schematic

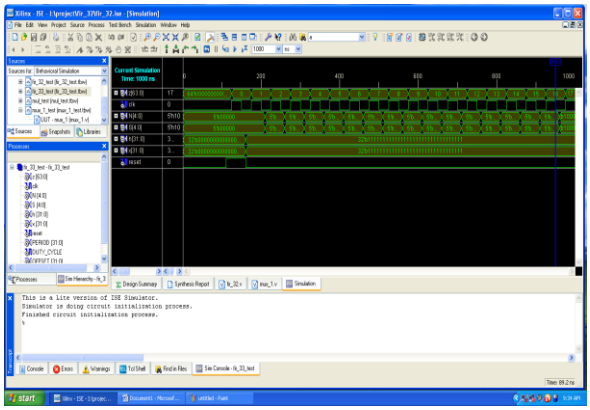

Figure: 5 32Tap FIR filter Simulation Results

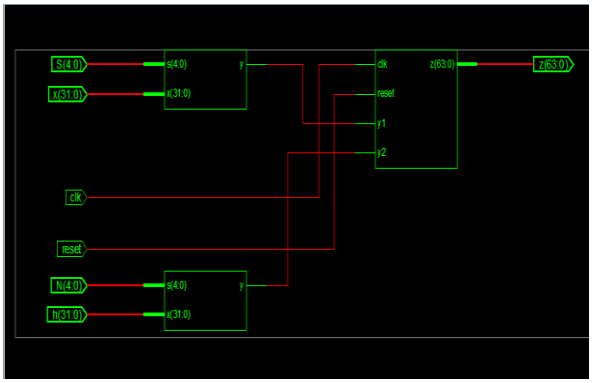

Figure 6: 32 Tap FIR filter RTL schematic

VI. CONCLUSION

In this paper we have approached new concept of designing single MAC unit based finite impulse response filter using FPGA. We have designed 8 and 32 coeffients FIR filter successfully with reduced latency. We have used fastest MAC unit for designing FIR filter, thus yielding high speed. The figures show the simulation results with reduced latency.

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